A Sliding-Mode Controller with Zero Forced Zero PWM for Full Bridge Inverter

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***Abstract*—Sliding mode control scheme for the full bridge inverter was analyzed, including modeling the variable structure system, selecting the switching line and control law. To make maximum use of degrees of freedom of the full bridge inverter circuit switching device, the idea of the single polarity sine pulse width modulation (SPWM) is introduced to the sliding mode control in full bridge inverter to reduce the switching loss. Furthermore, zero forced zero sliding mode PWM is used to suppress voltage distortion caused by sliding mode surface passing zero modulation. Simulation results are given to verify the correctness and validity of implemented zero forced zero sliding mode PWM for full bridge inverter.**

***Index Terms*—sliding mode control, full bridge inverter, variable structure system, pulse width modulation.**

I. Introduction

In recent years, sliding mode control method gradually attracted the attention of scholars [1]. Its biggest advantage is that sliding mode has fully adaptive to interference and perturbation on the system, and once the system state enters into the sliding mode motion, it quickly converges to the control objective [2]-[4].

As the power conversion device for DC/AC, Inverter has become an indispensable electrical device for production and living. Such as UPS, AC motor drives and car adapter, etc [1], [3]. The design of this kind of inverters requires high efficiency, highly stable output voltage and low harmonic distortion [5]-[7]. At the same time it should be considered that the inverter output has rapid dynamic property and stable robustness in the case of unstable input voltage and frequent load change [8]-[10]. Normally the inverter adopts SPWM to guarantee the low distortion of the output voltage waveform, and stabilizes the output voltage amplitude by the output voltage RMS feedback and routine control [11]-[13]. But this control method needs longer time to recover when facing the load change and its dynamic property is rather poor. Especially when there are intermediate requirements for the dynamic property of the inverter, it is difficult for the traditional control method to satisfy [1]-[4], [10]. Based on the variable structure system theory, sliding-mode control shows the insensitivity, robustness and good dynamic property for system parameters change and load change, which can be applied to control the inherent variable structure system of the inverter. Document [10] firstly applies sliding-mode control to single-phase inverter, and then gives the switching line and control action, and experimental results verify the advantage of sliding-mode control. Document [14] analyzes sliding-mode control inverter systematically. These can show that sliding-mode control inverter has good dynamic property and robustness. Furthermore, many sliding-mode methods are analyzed for inverter [1]-[4], [15]-[16].

This paper conducts a research on the key design technology of sliding-mode control full bridge inverter, and sets up the variable structure model, determining switching line and switch control law. To make maximum use of degrees of freedom of the full bridge inverter circuit switching device, the idea of the single polarity sine pulse width modulation (SPWM) is introduced to the sliding mode control in full bridge inverter to reduce the switching loss. Furthermore, zero forced zero sliding mode PWM is used to suppress voltage distortion caused by sliding mode surface passing zero modulation. Simulation results are given to verify the correctness and validity of implemented zero forced zero sliding mode PWM for full bridge inverter.

II. The Mathematical Model of Full Bridge Inverter

Power conversion circuit structure of the full bridge inverter is shown in Fig. 1. Inverter can generate three different phase voltage u_{inv}(+E, 0 and -E) through four switch (Q1, Q2, Q3, Q4) with different sets of switch connected the dc power supply to the ac output side. When Q1 and Q3 are turned on, it gives u_{inv}=+E. When Q2 and Q4 are turned on, it gives u_{inv}=-E. When Q1, Q2 or Q3, Q4 are turned on, it gives u_{inv}=0. The relationship between output level and switch state is shown in Table I. Switch state '1' means the switch is on and '0' means the switch is off.

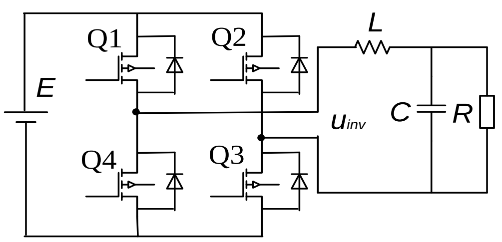

Figure 1. The Structure of full bridge inverter.

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TABLE I. THE RELATIONSHIP BETWEEN OUTPUT LEVEL AND SWITCH STATE.

u_{inv}	Q_1	Q_3	Q_4	Q_2	Output condition
E	1	1	0	0	P
0	0	1	1	0	O
	1	0	0	1	
-E	0	0	1	1	N

Ac square wave voltage output is converted to sinusoidal output voltage by the LC low pass filter. Output filter capacitor voltage and its derivative are continuous measurable, so capacitor voltage and its derivative are regarded as phase variables of the system to describe the system. System state equation is shown in Eq. (1).

$$\begin{bmatrix} \dot{u}_c \\ \ddot{u}_c \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -1/LC & -1/RC \end{bmatrix} \cdot \begin{bmatrix} u_c \\ \dot{u}_c \end{bmatrix} + \begin{bmatrix} 0 \\ E/LC \end{bmatrix} \cdot u \quad (1)$$

where $u \in \{1,-1\}$, while u=1, u_{inv}=E; while u=-1, u_{inv}=-E.

Eq. (1) can be used as a variable structure model of the full bridge inverter. The derivative of output capacitor voltage can be got by capacitor voltage and capacitance current as shown in Eq. (2).

$$\dot{u} = i / C \quad (2)$$

Thus, as long as the reference output signal is known, the difference between the reference signals and state variables can be regarded as a new state variables. So system state equation is shown in Eq. (3).

$$\begin{bmatrix} \dot{V}_{ref} - \dot{u}_c \\ \ddot{V}_{ref} - \ddot{u}_c \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -1/LC & -1/RC \end{bmatrix} \cdot \begin{bmatrix} V_{ref} - u_c \\ \dot{V}_{ref} - \dot{u}_c \end{bmatrix} + \begin{bmatrix} 0 \\ -E/LC \end{bmatrix} \cdot u + \begin{bmatrix} 0 \\ \ddot{V}_{ref} + \dot{V}_{ref}/RC + V_{ref}/LC \end{bmatrix} \quad (3)$$

III. THE SLIDING MODE CONTROL OF FULL BRIDGE INVERTER

On the phase plane as shown in Eq. (3), a straight line, which get through the origin with negative slope is selected as switch line, namely:

$$\delta(u_c, t) = k_1[V_{ref}(t) - u_c] + k_2[\dot{V}_{ref}(t) - \dot{u}_c] = 0 \quad (4)$$

The structure diagram of sliding mode control is shown in Fig. 2. In order to make the system state trajectory along the slide switch line and eventually stable at the origin, k1 and k2 are ensured to be positive, i.e. $k_1 > 0$, $k_2 > 0$. On the switch line, dynamic sliding mode area is a first order dynamic process as shown in Eq. (4). Solution to the output voltage Uc(t) for dynamic process is:

$$u_c(t) = V_{ref}(t) + \mu \cdot e^{-k_1 t / k_2} \quad (5)$$

The dynamic process of the output voltage of inverter working in sliding mode surface is determined by the ratio (k1/k2) of the switching surface coefficient and the initial state (μ) when the state trajectory reach the switching surface, and has nothing to do with the other parameters of the system, which embodies the robustness of sliding state system to external disturbance and change of internal parameters. Due to the variable structure system described by Eq. (1) includes two subsystems, each has a unique equilibrium point. As long as the switching line make balance point respectively in its two sides and system equilibrium point is located in the opposite side of switch line, the switch line is accessible. As a result, control function is as follows:

$$u = \begin{cases} +1, \delta > 0 \\ -1, \delta < 0 \end{cases} \quad (6)$$

While $\dot{\delta} = 0$, the corresponding equivalent control is as follows:

$$u_{eq}(t) = \frac{LC}{E}\left[\ddot{V}_{ref} + \lambda \dot{V}_{ref} + \left(\frac{1}{RC} - \lambda\right)\dot{u}_c + \frac{1}{LC}u_c\right] \quad (7)$$

where $\lambda = k_1 / k_2 > 0$.

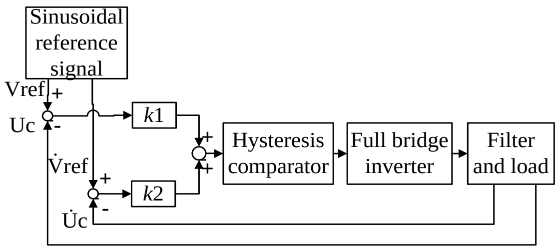

Figure 2. Block diagram of sliding mode control.

IV. SINGLE POLARITY SLIDING MODE PWM

For full bridge inverter circuit, inverter output voltage using single polarity SPWM has only zero level and a positive or negative level in each switch cycle, which makes two switching devices in the conduction on or off state for a long time, reducing the switch losses and output voltage jump. To make maximum use of degrees of freedom of the full bridge inverter circuit switching device, the idea of the single polarity SPWM will be introduced to the sliding mode control in full bridge inverter. In Fig. 1, in the process of the whole modulation, a switch tube can be kept conducting, and another switch tube in the high frequency switch state. When P state is needed for output in Table I, Q1 has been in the conducting state and Q3 can be modulated by the sliding mode controller; When P status is needed for output in Table I, Q2 has been in the conducting state and Q4 can be modulated by the sliding mode controller. As shown in Fig. 3, drive pulse waveforms (ug1, ug3) of switch tube (Q1, Q3) is compared. Thereinto, ug1 is power frequency square wave, and ug3 is got by the switch function as Eq. (8).

$$u_{g3} = \begin{cases} 1, \delta > 0 \\ 0, \delta < 0 \end{cases} \quad (8)$$

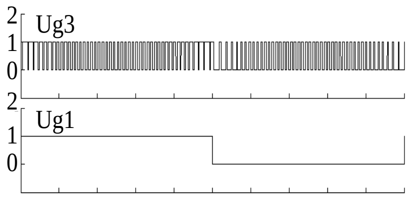

Figure 3. Drive pulse waveform (ug1, ug3) of switch tube (Q1, Q3).

A problem exists in the process of single polarity sliding-mode PWM control as shown in Fig. 4. When the sinusoidal output voltage each passes zero, the two low frequency switches of full bridge inverter need switch over, namely, ug1 and ug4 drive pulse signal switching between 0 and 1. If the other two high frequency switches have not yet returned to the sliding surface at this time, modulation will have a big deviation. For example, when the sinusoidal output voltage is passing zero potential from positive to negative, i.e. ug1 changed from 1 to 0, ug4 changed from 0 to 1. If the ug2, ug3 did not return to the sliding mode surface, i.e. they keep on pulse condition of the moment before. At the same time, if the ug2 is 1, ug3 is 0. In this way, ug2 and ug4 is conducting state, as a result the output is -E, which can be got from Table I. According to the principle of PWM modulation, when sinusoidal output pass the zero point, modulation pulse needed should be 0, otherwise the output voltage distortion happens.

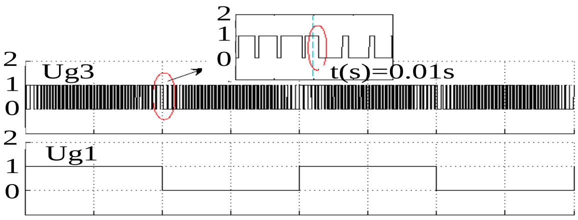

Figure 4. Single polarity sliding-mode PWM directly.

In order to solve the above problems, zero forced zero sliding-mode PWM is used to suppress voltage distortion caused by this kind of sliding mode surface passing zero modulation. Every time when sinusoidal output voltage pass zero, the other two drive pulse of high frequency switch devices (ug2, ug3) are forced to 0. Thus,

$$\begin{cases} u_{g3}' = u_{g3} * u_{gx} \\ u_{g2}' = u_{g2} * u_{gx} \\ u_{g1}' = u_{g1} \\ u_{g4}' = u_{g4} \end{cases} \tag{9}$$

where u_{gx} is square wave signal, the duty cycle is determined by sampling period (T_s).

There is a further discussion about time of zero forced zero. If time of zero forced zero is too short, it may result in the incomplete elimination for sliding mode surface passing zero modulation, thus the surplus and even the opposite modulating pulse will result in the distortion of the output voltage; If time of zero forced zero is too long, it may influence the successive half cycle of normal sliding mode PWM. After analyzing, it is found that the influence time of sliding mode surface passing zero modulation will be a switch cycle at most, so time of zero forced zero can be determined.

V. Simulation Results

In order to verify the correctness and validity of implemented zero forced zero sliding mode PWM for full bridge inverter in this paper, the simulation is investigated under the environment of Matlab/Simulink. The specific circuit and the control parameters are as follows:

The input voltage: E=60V;

Filter parameters and the rated load: L=500µH, C=20µF, R=40Ω;

The sliding coefficient: k_1=12,k_2=0.005;

Hysteresis width and switching frequency: $2h$=20,f_s=5kHz.

Fig. 5 is pulse waveform of single polarity sliding-mode PWM directly. In 0.01s and 0.02s, which is half a power frequency cycle, ug2 and ug3 will take sliding mode surface passing zero modulation. Fig. 6 is pulse waveform of zero forced zero single polarity sliding-mode PWM. Obviously, sliding-mode surface zero modulation pulse is removed in ug2 and ug3, becoming zero immediately after 0.01s or 0.02s.

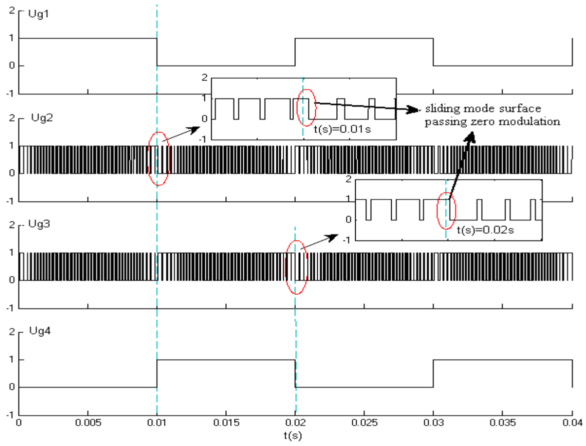

Figure 5. Pulse waveform of single polarity sliding-mode PWM directly.

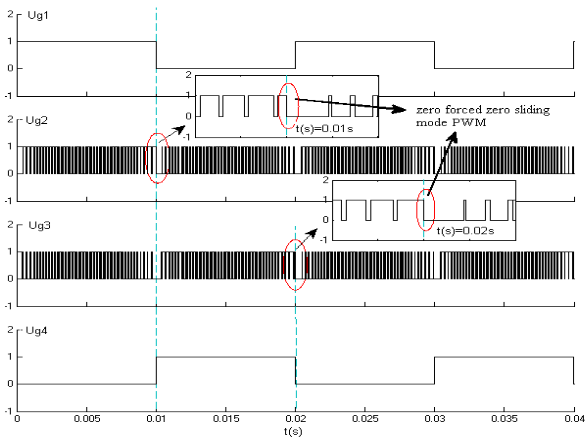

Figure 6. Pulse waveform of zero forced zero single polarity sliding-mode PWM.

Fig. 7 is inverter output voltage while using direct single polarity sliding-mode PWM. Under the influence of the sliding mode surface zero modulation pulse, excess dc voltage pulse exist in u_{inv} at 0.01s and 0.02s. Fig. 8 is inverter output voltage while using zero forced zero single polarity sliding-mode PWM. According to the principle of PWM modulation, sinusoidal modulation pulse should need 0 when the output passed zero. The inverter output voltage (u_{inv}) is zero after 0.01s and 0.02s instant.

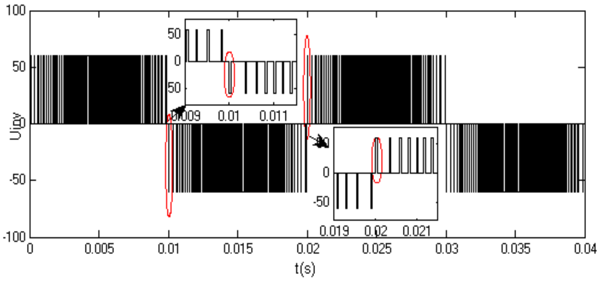

Figure 7. Inverter output voltage while using direct single polarity sliding-mode PWM.

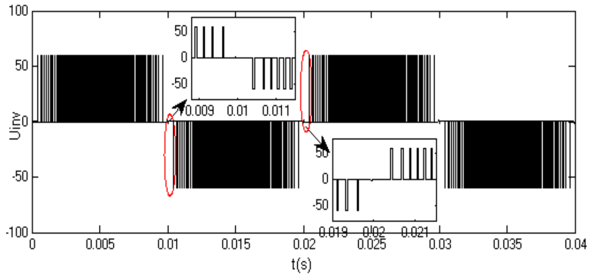

Figure 8. Inverter output voltage while using zero forced zero single polarity sliding-mode PWM.

Fig. 9 is load voltage waveform while using direct single polarity sliding-mode PWM and THD analysis. Obviously, load voltage have extreme voltage distortion at 0.01s, 0.02s, THD is quite high. Fig. 10 is load voltage waveform while using zero forced zero single polarity sliding-mode PWM and THD analysis. Contrast, the zero forcing zero single polarity sliding-mode PWM can make the output voltage waveform approximate sine wave, and decrease THD to 15.45% from 18.77%.

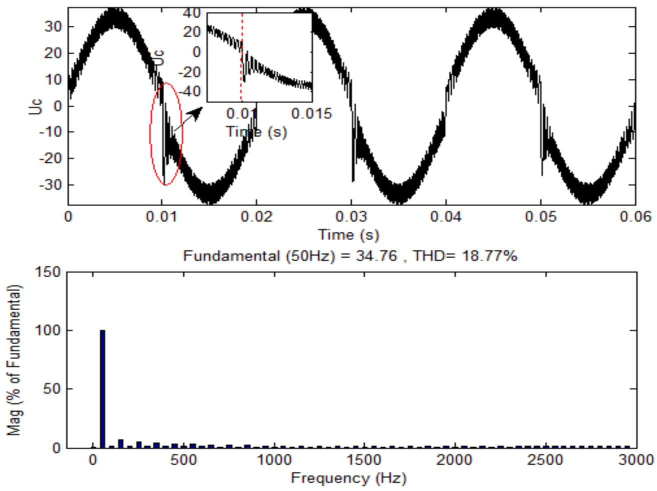

Figure 9. Load voltage waveform while using direct single polarity sliding-mode PWM and THD analysis.

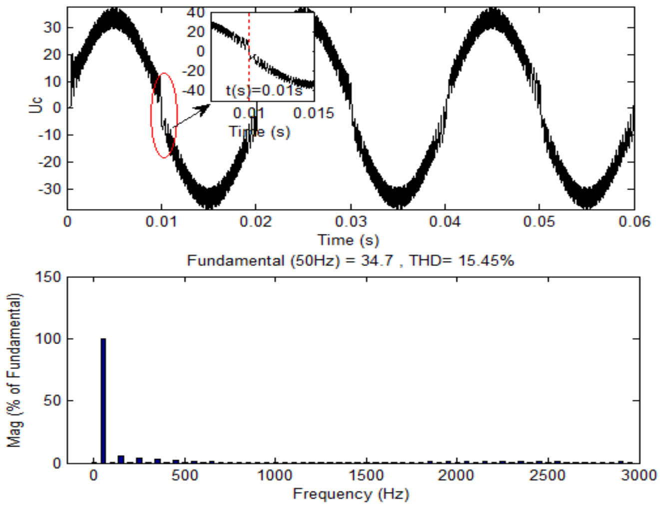

Figure 10. Load voltage waveform while using zero forced zero single polarity sliding-mode PWM and THD analysis.

VI. Conclusion

A sliding mode control scheme for the full bridge inverter was analyzed, including modeling the variable structure system, selecting the switching line and control law. To make maximum use of degrees of freedom of the full bridge inverter circuit switching device, the idea of the single polarity sine pulse width modulation is introduced to the sliding mode control in full bridge inverter to reduce the switching loss. Furthermore, zero forced zero sliding mode PWM is used to suppress voltage distortion caused by sliding mode surface passing zero modulation. Simulation results have verified the correctness and validity of implemented zero forced zero sliding mode PWM for full bridge inverter.

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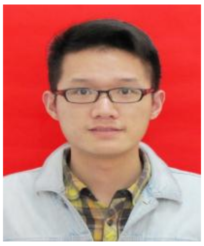

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