Design Analysis and Performance Comparison of Low Power High Gain 2nd Stage Differential Amplifier Along with 1st Stage

Sadeque Reza Khan
Department of Electronic and Communication Engineering, National Institute of Technology, Karnataka, India
Email: sadeque_008@yahoo.com

***Abstract*—The CMOS differential amplifier with active load and single-ended output is one of the most popular circuits used in analog and mixed signal applications owing to its amazing performances. In this paper an op-amp of 2nd stage is designed for certain specifications such as gain and slew rate and its comparison analysis with a 1st stage is realized. The proposed classic two-stage op amp produces an open loop gain above 70 dB, gain- bandwidth product (GBW) of 11.43 MHz and 50.4^{o} phase margin in 0.60 µm CMOS technology. The circuit is operated at the supply voltage of 3.3 V with power dissipation of 144.3 µW. The ability of the method adopted, to use the smaller compensation capacitor, Cc, which improves the slew rate, also beneficial for the area of compensation circuit.**

***Index Terms*—gain bandwidth; slew rate; input common mode; common mode rejection ratio; power supply rejection ratio**

I. Introduction

Among the basic analog circuits, differential amplifiers play a very important role because of their excellent performances as input amplifiers and the straightforward application possibility of feedback to the input [1], [2]. Active load and single ended output differential amplifier is the most common version of the differential amplifier in CMOS analog circuits [3]. This circuit has amazing features in terms of self-bias capability, common-mode rejection, voltage gain, and the gain-bandwidth product. The goal of this paper is to design a two-stage CMOS operational amplifier with low power dissipation and high gain by using AMI C5N 0.6 µm technology and analyze the performance comparison of 2nd stage with the 1st stage op-amp. The design methodology followed in this paper is to propose straightforward yet accurate equations for the design of high-gain two staged CMOS op-amp and for doing so, a simple analysis with some meaningful parameters (phase margin, gain-bandwidth, *etc*.) is performed. The schematics and simulations in this paper were carried out in the Cadence Environment.

II. Architecture and Operation

The two-stage CMOS operational amplifier in this paper includes four major circuitries—a bias circuit, a 1st stage differential amplifier, a second gain stage, a compensation circuit which is shown in figure 1. In a classic op amp architecture, the first stage usually consists of a high-gain differential amplifier which includes the most dominant pole of the system. A common source amplifier usually meets the specification of second stage, having a moderate gain. The third stage is most commonly implemented as a unity gain source follower with a high frequency and negligible pole [4]. Differential amplifiers are often desired as the first stage in an op amp due to their differential input to single ended output conversation and high gain [5] and the second stage implementation can increase gain but this stage is mostly desirable for high output swing. Again higher gain leads to lower bandwidth and the designer has to decide between these tradeoffs based on the specifications of the system and user requirements.

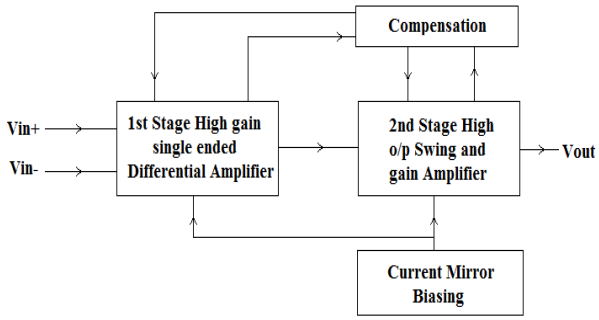

Figure. 1. Block diagram of a two-stage operational amplifier

The Bias Circuit is provided to establish the proper operating point for each transistor in its saturation region. The purpose of the Compensation Circuit is to maintain stability when negative feedback is applied to the op amp. A typical circuit configuration of an un-buffered two-stage op amp (including the Input Differential Amplifier and the Second Gain Circuit) is shown in Figure 2 where transistors M1, M2, M3, and M4 form the first stage of the op amp—the differential amplifier with differential to single ended transformation [6]. The second stage is a current sink load inverter where M6 is the driver while M7 acts as the load. Capacitor Cc is used to lower the gain at high frequencies and provide the compensation for

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the op amp to provide the proper stability of the amplifier. The first stage and the second stage circuits use the same reference current; hence, the bias currents in the two stages are controlled together.

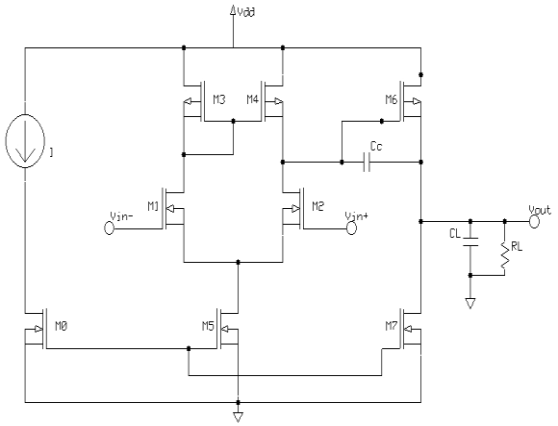

Figure. 2. Circuit configuration for a two-stage op amp with an n-channel input pair

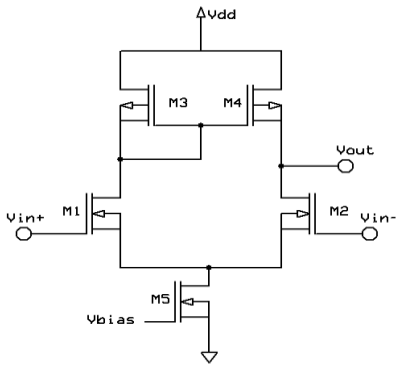

Figure 3. Circuit Configuration for a one-stage op amp

III. Specifications and Design Procedure

The design in this paper is a two-stage op amp with an n-channel input pair. The op amp uses a single-polarity power supply (Vdd and Gnd). Based on the SPICE parameters of AMI C5N 0.6 μm technology, the topology was determined to achieve the specifications listed below in Table I and Table II:

Table I: Boundary Conditions for the CMOS op Amp

Boundary Conditions	Requirements
Supply Voltage	0-3.3 V
Temperature	0-70 o C

Table II: Specifications for the CMOS op Amp

Specifications	Proposed Value
Gain	≥ 70dB
Gain Bandwidth (GB)	≥ 10MHz
3dB BW	≥ 1.5KHz
Phase Margin	≥45 o
Slew Rate	≥ 5 V/μs
Settling Time	≤ 1μs
ICMR	1.5 – 2.5 V
CMRR	≥ 50dB
PSRR	≥ 100dB
Output Swing	0 – 3.3V
Power Dissipation	≤ 2mW

The steps that are followed in designing the op-amp are given bellow [7]:

1) *The compensation capacitance is chosen to be at least 0.22 times the load capacitance Cc > 0.22CL.*

Here Cc is the compensation capacitance and CL is the load capacitance.

2) *Determine the value for the "tail current"* (I_5).

$I_5 = SR .Cc$

Here SR is the slew rate of the op-amp.

3) *Design for* M_3 *from the maximum input voltage specification.*

$$M_3 = (I_5 \div K_3 [V_{DD} - V_{IN\,(max)} - V_{TO3\,(max)} + V_{T1\,(min)}]^2)$$

I_5 is the drain current of M_5, V_{DD} is the positive supply voltage, V_{IN} is the input voltage, V_T is the threshold voltage and K is the transconductance parameter (in saturation).

Also, M = (W/L).

4) *Design for* M_1 (M_2) *to achieve the desired GB.*

$$g_{m1} = g_{m2} = GB.\ Cc$$
$$M_2 = 2g_{m2} / K_2\ I_5$$

GB is the gain bandwidth and g_m is the small signal transconductance from gate to channel.

5) *Design for* M_5 *from the minimum input voltage. First calculate* V_{DS5} *(sat) then find* M_5.

$$V_{DS5}\,(sat) = V_{IN}\,(min) - V_{SS} - \sqrt{(I_5/\beta_1)} - V_{T1}\,(max)$$
$$M_5 = 2\ I_5 / K_5\ [V_{DS5}\,(sat)]^2$$

where, β is the MOS transconductance parameter and V_{SS} is the negative supply voltage.

6) *Find* g_{m6} *and* M_6.

$$g_{m6} = 2.2\ g_{m2}\,(C_L/Cc)$$
$$M_6 = M_3\,(g_{m6} / g_{m3})$$

7) *Calculate* I_6:

$$I_6 = (M_6/M_4)\ I4 = (M_6/M_4)\ (I_5/2)$$

8) *Design S7 to achieve the desired current ratios between I5 and I6.*

$$M_7 = (I_6/I_5)\ M_5$$

From the above equations the retrieved value of different MOSFET are as follows in Table III:

Table III: Calculated Size of Different MOSFETS

Device	Type	Calculated Size	Ratio
M5	NMOS	2.6 μm / 0.6 μm	4.38
M1,M2	NMOS	6.6 μm / 0.6 μm	11
M3,M4	PMOS	3.36 μm / 0.6 μm	5.6
M6	PMOS	58.8 μm / 0.6 μm	98
M7	NMOS	22.8 μm / 0.6 μm	38
C_C	Compensating Capacitor	3pF	
C_L	Load Capacitor	10pF	

Table IV. Simulated Size of Different MOSFETs

Device	Type	Simulated Size	Ratio
M5	NMOS	1.5 μm / 0.6 μm	2.5
M1,M2	NMOS	32 μm / 1.5 μm	21
M3,M4	PMOS	8.4 μm / 1.5 μm	5.6
M6	PMOS	100 μm / 1.5 μm	66
M7	NMOS	9.45 μm / 1.5 μm	6.3
C_C	Compensating Capacitor	2.7pF	
C_L	Load Capacitor	5pF	

IV. Simulation Results and Comparison with 1st Stage Performance

Practical size of MOSFET retrieved from the simulation results are given bellow in Table IV:

A. Frequency Response

The open-loop gain, gain bandwidth, cut-off frequency, and phase margin were obtained by using ac frequency sweep analysis. Here for the 1st stage the open loop gain is 40.48dB and phase is 88.65 ° but gain bandwidth is 6.855MHz which is very low indeed. Again the open-loop voltage gain is 73.03dB where the gain starts to cut off around 2.71 KHz (the -3dB frequency) for the 2nd stage. The gain bandwidth is 11.43MHz (the unity gain frequency, 0dB). The phase margin for a 5pF load is 50.4 ° which is a moderate figure. The frequency response curve for the 1st and 2nd stage are shown in the Fig. 4 and Fig. 5 respectively.

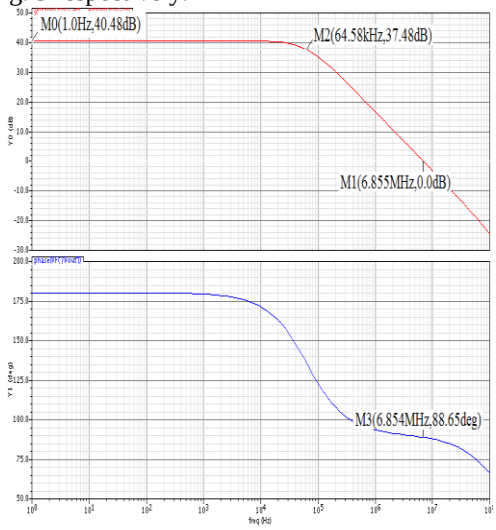

Figure. 4. Frequency response simulation result for 1st stage

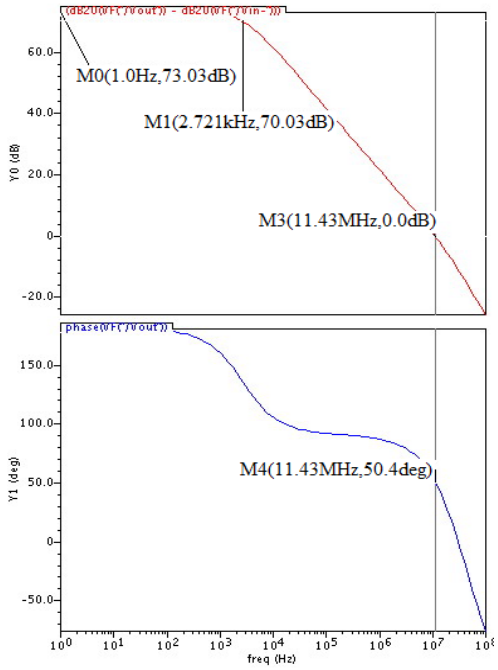

Figure. 5. Frequency response simulation result for 2nd stage

B. Slewing and Settling Time

The positive slew for the 1st stage op amp is 1.70V/µs and the negative slew is -1.54V/µs which is very poor performance and the setting time is 0.97us. Whereas the 2nd stage positive slew rate is 5V/µs and the negative slew rate is –4.7V/µs for both simulations. The settling time is 0.25µs faster than the proposed specification 1µs for schematic simulation.

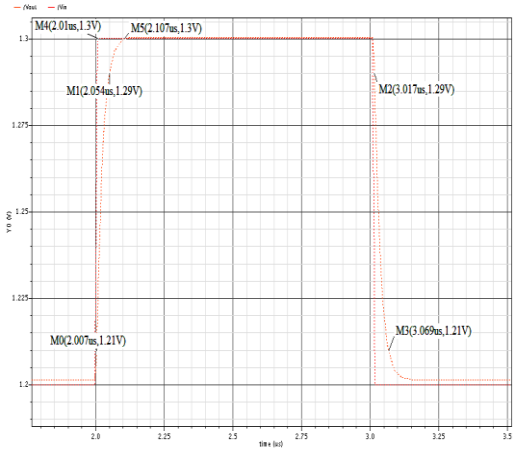

Figure. 6. Slew and Settling time simulation result for 1st stage

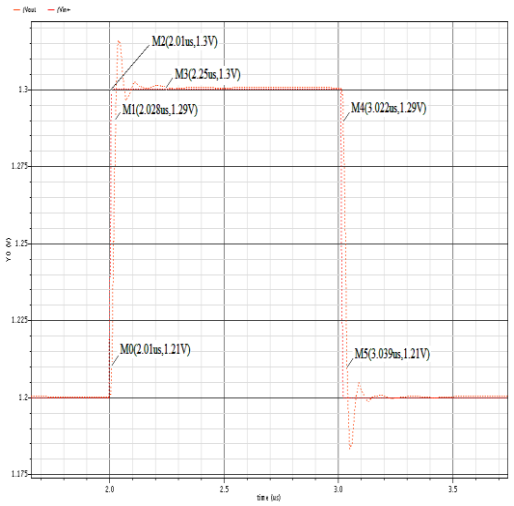

Figure. 7. Slew and Settling time simulation result for 2nd stage

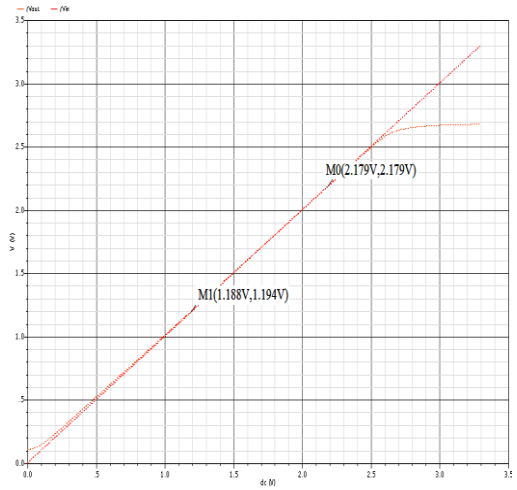

Figure. 8. ICMR for 1st stage

C. Input Common Mode Range (ICMR)

The ICMR for schematic simulation for 1st and 2nd stage(shown in Fig. 8 and Fig. 9) is from 1.188V to 2.179V and 0.3V to 2.52V respectively, which has wider range than the proposed specification of ICMR (1.5 ~ 2.5V) where 1st stage range is lower than the specification.

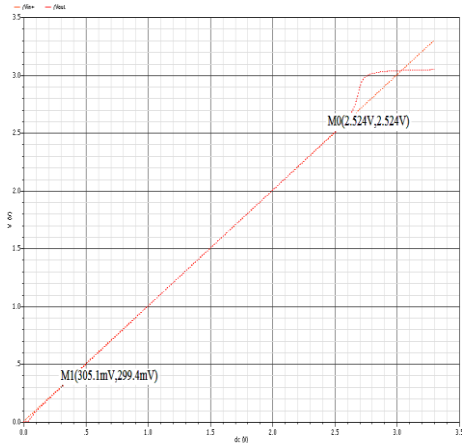

Figure. 9. ICMR for 2nd stage

D. Common Mode Rejection Ratio (CMRR)

The common mode rejection ratio measures how the output changes in response to a change in the common-mode input level. Ideally, the common mode gain of an Op amp is zero. Common Mode Rejection for 1st stage is 55.27 DB and 2nd stage is 51.5dB which is very close to 1st stage.

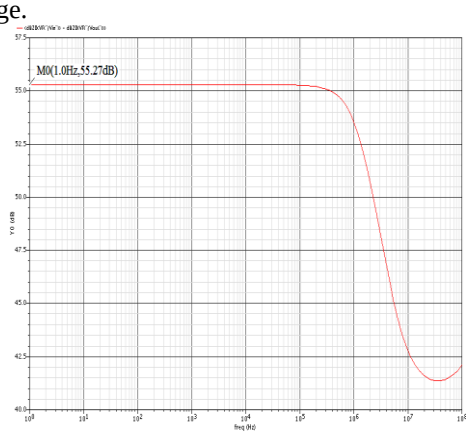

Figure. 10. CMRR for 1st stage

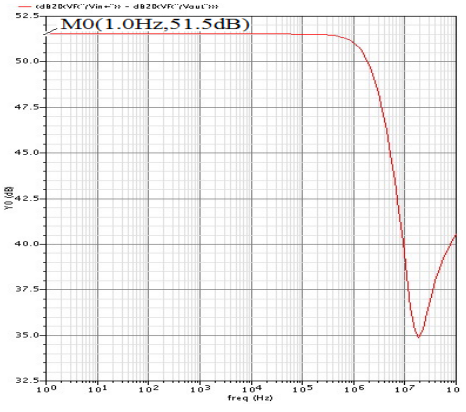

Figure. 11. CMRR for 2nd stage

E. Power Supply Rejection Ratio (PSRR)

It is used to measure amount of noise rejection probability by the amplifier enforced by the power supply. A small sinusoidal voltage is placed in series with V_{dd} to measure PSRR, which are 54.35dB for 1st stage and 109.3 dB for 2nd stage.

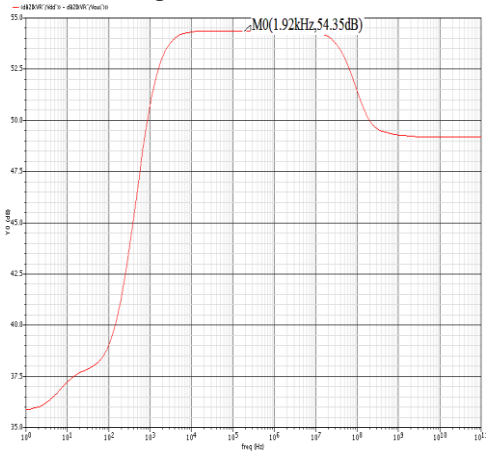

Figure. 12. PSRR for 1st stage

F. Output Swing and Power Dissipation

The output swing simulation can be obtained by using a configuration of close-loop inverting gain. The output voltage swing of the amplifier of 1st stage is 407.5mV to 3.29V and 182.4 μV to 3.24V.

Through DC sweep analysis on the voltage source at the inputs of the 2nd stage op amp, the power dissipation is around 0.74mW for the low DC input with 0.3 V and 1.23mW for the high DC input with 3.3V. The DC sweeps from -1.8V to 3.3V due to the ICMR of the op amp.

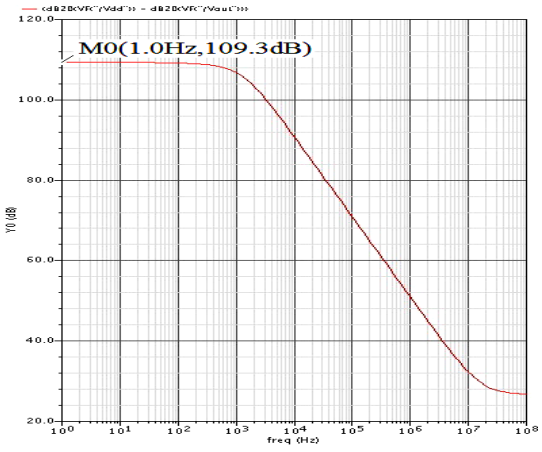

Figure. 13. PSRR for 2nd stage

G. Summary

Table V shows the simulation results extracted from the schematic and also shows some similar reference results.

TABLE V: COMPARISON OF THE DESIRED SPECIFICATIONS AND THE SCHEMATIC SIMULATION RESULTS

Specifications	Schematic Simulation	[8]	[9]	[3]

Technology	0.6 µ	2 µ	0.5 µ	0.35 µ
Supply Voltage	3.3V	5V	5V	5V
Gain	73.03dB	84dB	48.8dB	77.25dB
Gain Bandwidth (GB)	11.43MHz	6 MHz	9.32 MHz	14.1 MHz
3dB BW	2.71KHz	-	-	1.3KHz
Phase Margin	50.4^{o}	50^{o}	93.14^{o}	85.85^{o}
Slew Rate	5V/µs	-	36 V/ µs	10.33 V/ µs
Settling Time	0.25µs	-	0.163 µs	0.4 µs
ICMR	0.3 - 2.52V	-	-	0.9-3.24V
CMRR	51.5dB	-	-	80.98dB
PSRR	109.3dB	-	-	-
Output Swing	182.4µV-3.24V	-	1.75V-4.86V	0.0V-3.28V
Power Dissipation	1.23mW	54.36mW	4.88 mW	-

V. Conclusion

This paper presents the full custom design of a two stage fully differential amplifier with active load and single ended output where biasing is done by perfectly matched current mirror circuit; both the hand calculations and computer-aided simulation results are given in detail. The results show that the designed amplifier has successfully satisfied all of the specifications given in advance and also held the characteristics of a good op amp. Especially, with the optimal design procedure and specific techniques, the amplifier reaches very large output swing and fast settling time. In addition, the open loop amplifier also has a considerably high gain with very low power consumption at the instant of full swing operation.

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Sadeque Reza Khan received B.Sc. degree in Electronics and Telecommunication Engineering from University of Liberal Arts Bangladesh and continuing his M.Tech in VLSI from National Institute of Technology Karnataka (NITK), India. Currently he is in study leave from his Institution where he was working as a lecturer in the department of Electrical and Electronic Engineering in Prime University, Bangladesh. His research interest includes VLSI, Microelectronics, Control System Designing and Embedded System Designing.