Comparative Evaluation of Performance Improvement in Capacitor-Supported Dynamic Voltage Restorer for Linear & Non-Linear Loads

S. P. Gawande
Yeshwantrao Chavan College of Engineering, Department of Electrical Engineering, Nagpur, India
Email: spgwande_18@yahoo.com

M. R. Ramteke
Visvesvaraya National Institute of Technology, Department of Electrical Engineering, Nagpur, India
Email: mrramteke@rediffmail.com

***Abstract*—The main aim of DVR is to regulate the voltage at load terminals irrespective of any power quality problems like sag, swell, distortion or unbalance in load or supply voltage. This paper presents the dynamic performance characteristics of a Dynamic Voltage Restorer (DVR) that protect balanced, unbalanced as well as sensitive loads. Also different DVR configurations are suggested which do not supply or absorb any active power during the steady state operation. The DVR operation is verified though MATLAB simulation using simulink blocksets.**

***Index Terms*—Custom power device, dynamic voltage restore, unbalanced load, non-linear load, voltage source inverter**

I. Introduction

A dynamic voltage restorer (DVR) is a power electro-electronics converter-based series connected custom power device that can protect critical loads from most common supply side disturbances. The basic operating principle of a DVR is to inject a voltage of required magnitude and frequency in series with a distribution feeder to restore the voltage on the load side to the desired amplitude and waveshape even when supply voltage is unbalanced or distorted [1]. Usually pulse width modulated (PWM) voltage source inverter (VSI) employing IGBT or GTO along with or without energy storage systems (ESS) realizes a DVR. The output of the VSI is connected in series with a distribution feeder through a transformer. The VSI can be supplied by dc source. With this, the DVR can regulate the load voltage at any given magnitude and phase angle. This can be accomplished through real power exchange between the dc source and the ac system through the inverter. However, during load rejection, the excess power must be returned to the ac lines. In real situation when the dc bus of the DVR is supplied through the rectifier, the reverse power flow may damage the rectifier unit if the phase angle of the desired load bus voltage is less than that of the terminal voltage [2]. Also such ac supported DVR is relatively expensive and needs additional control for rectifier.

In this paper, a general method; adopting different DVR configurations is proposed to maintain balanced sinusoidal load voltage with a desired magnitude at any load; while the average real power supplied or absorbed by DVR in steady state is zero.

The proposed scheme is validated through computer simulation using MATLAB Simulink. This paper also discusses the structure of DVR with different configurations using voltage source inverter supplied by the filter capacitor in shunt to DVR, at point of common coupling (PCC) & load.

II. DVR Structure

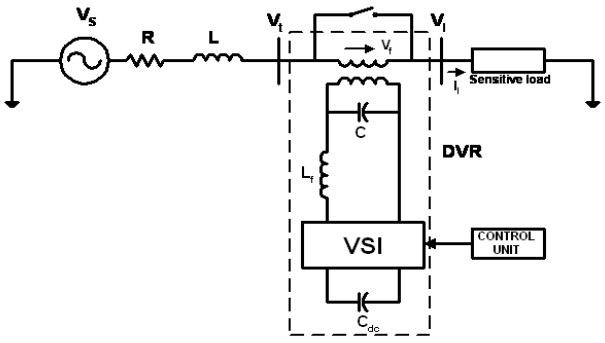

Figure 1. General schematic diagram of the DVR.

The DVR structure is shown in Fig. 1. It consists of 6-pulse VSI connected to a common dc storage capacitor (C_{dc}). The voltage V_{dc} across C_{dc} is the dc input to the inverter. The output of the inverter is connected to the single phase transformer. The outputs of the three transformers are then connected in series to the three respective phases of the distribution feeder. The single phase equivalent circuit of the DVR is shown in Fig. 2, in which L_d represents the leakage reactance of the transformer and R_d represents the losses in the inverter

Manuscript received December 2, 2012; revised December 15, 2013.

doi: 10.12720/joace.1.4.353-357

circuit [2]-[3]. The term uV_{dc} represents the inverter output voltage where V_{dc} is the voltage across the dc capacitor and u is the switching function. From Fig. 2, we get the following relation:

$$V_f = u.V_{dc} - R_d i_1 - L_d \frac{di_1}{dt}. \quad (1)$$

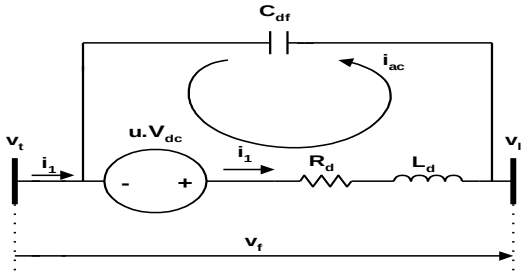

Figure 2. Single-phase equivalent circuits of the DVR with shunt filter capacitor.

III. Components Of Distribution System

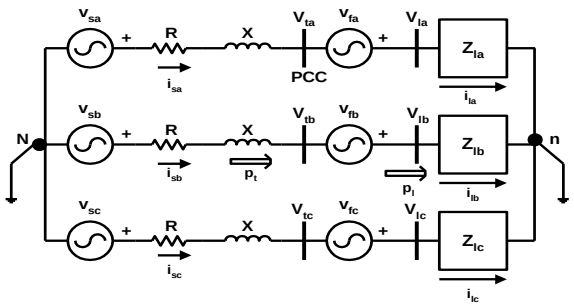

Figure 3. Schematic diagram of a series compensator connected power system.

The schematic diagram of series compensator connected power system is shown in Fig. 3. In this, the DVR is connected in series between the PCC and the load. With respect to above series compensated distribution system following are the system components.

- Instantaneous supply voltages: V_{sa}, V_{sb}, and V_{sc}.
- Line currents or Load currents: i_{sa}, i_{sb}, and i_{sc}.
- Series compensator as voltage source: Instantaneous voltage sources V_{fa}, V_{fb}, and V_{fc}.
- Terminal voltages: Instantaneous voltages V_{ta}, V_{tb}, and V_{tc}.
- Load voltages: Instantaneous voltages V_{la}, V_{lb}, and V_{lc}.
- Sensitive loads: Impedances Z_{la}, Z_{lb}, and Z_{lc} (This load is realized using rectifier load)

where subscript a, b and c denotes the three individual phases.

The series compensator is connected between a terminal bus and a load bus. The voltage sources are connected to the series compensator terminals by a feeder with an impedance of $R_i + jX_i$. Initially we assume a balance load i, e.

$$Z_{la} = Z_{lb} = Z_{lc} = R_i + jX_i \quad (2)$$

DVR reference voltage generation

By applying KVL in Fig. 3.we get

$$V_t + V_f = V_l \quad (3)$$

The main aim of DVR is to make the load voltage positive sequence. Further the DVR should not supply or absorb any real power. To force V_l to be positive sequence, V_f must cancel the zero and negative-sequence components of V_t. In addition, the V_f should be such that the load voltage is regulated at a pre-specified value [4]-[6]. Since the DVR must operate in zero power mode, we get

$$P_{lav} = P_{tav} = V_{ta} i_{sa} + V_{tb} i_{sb} + V_{tc} i_{sc} \quad (4)$$

where $P_{lav}$the instantaneous power is supplied to the load and P_{tav} is the average value of the instantaneous power entering the terminal

Let us consider the phasor load voltage as $V_l = |V_l|$ at an angle θ where $|V_l|$ is a pre-specified magnitude and θ is an unknown angle to be computed. Since the load voltage is positive sequence, the average power to the load is also positive sequence. Hence we get

$$P_{lav} = |V_l||I_{l1}| \cos(\theta - \Phi) \quad (5)$$

where$|I_{l1}|$ is the phasor positive sequence component of the load current; Φ is the load phase angle.

Combining equation (4) and (5) we get

$$\theta = \cos^{-1}\left(\frac{P_{tav}}{|V_l||I_{l1}|}\right) + \Phi. \quad (6)$$

If $|V_l|$ is known, P_{tav} can be calculated from the instantaneous measurement of terminal voltage and load current. The rms phasor positive-sequence component of the terminal voltage can be extracted from the sampled values as detailed in [5] and thus θ can computed

Denoting the zero, positive and negative phasors by the subscripts 0, 1, and 2, respectively, these components are given by

$$\begin{vmatrix} I_{lo} \\ I_{l1} \\ I_{l2} \end{vmatrix} = \frac{\sqrt{2}}{T\sqrt{3}} \int_t^{t+T} \begin{vmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{vmatrix} \begin{vmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{vmatrix} e^{-j(wt-90)} dt \quad (7)$$

where $a = e^{j120^0}$ and T is the integration interval. The reference phasor sequence component of the DVR voltages (V_{fi}^*) can be obtained from (3) as follows.

$$V_{fo}^* = -V_{to}\,,\ V_{f1}^* = |V_l| \angle \theta - V_{t1} \text{ and } V_{f2}^* = -V_{t2} \quad (8)$$

If the inverse symmetrical component transformation of (8) is taken, it produces the reference phasor voltages for the DVR.

IV. Cases With Different Confurations of DVR

This section presents simulated results with the different configurations of DVR. Here the DVR is realized by voltage source inverter supplied by dc capacitor. By using the proper simulation parameters, the capacitor supported DVR is demonstrated for the following cases.

Case 1: Filter capacitor in shunt with DVR.

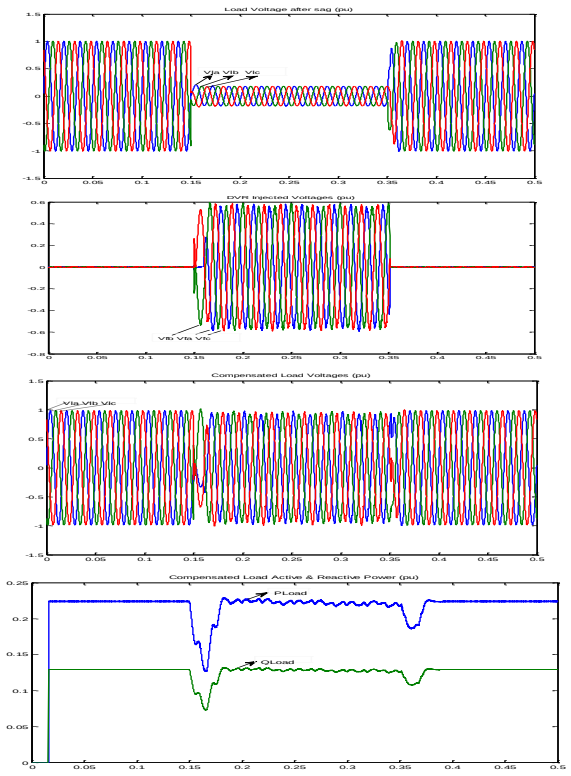

Figure 4. Load voltage after sag, DVR injected voltage, compensated load voltage, compensated active & reactive power of load.

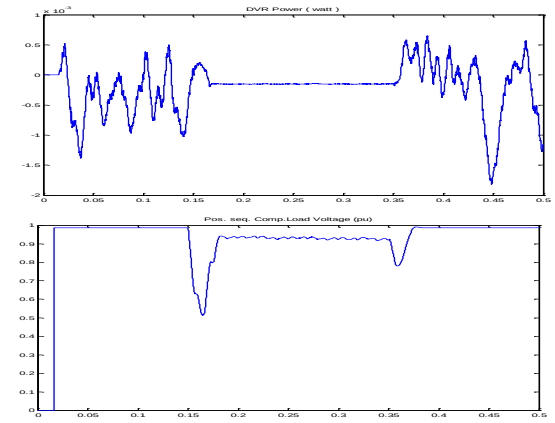

Figure 5. DVR active power, positive sequence component of load voltage.

In case 1 the DVR is connected with filter capacitor C_{df} in shunt as shown in Fig. 2. The 80% sag is observed with the balanced linear load. The DVR injects a balanced voltage for duration of 0.2 sec in order to compensate the sag & make the terminal voltage and load voltage 1.0 pu. As shown in Fig.4. It is seen that the DVR power oscillates close to zero & load power are compensated as shown in Fig. 4-5.

Case 2: DVR with Filter capacitor in shunt with PCC

In case-2, a non-linear load is introduced in addition to balanced linear load. The non-linear load is realized by using rectifier load. To accommodate this load, it is necessary to modify the DVR structure by putting additional shunt capacitor at PCC. Due to non-linear load the harmonic in the load current will distort the terminal voltage [7]-[12]. Since DVR only cancels the negative and zero sequences, the harmonic components of the terminal voltage will pass on to the load voltage. Hence the terminal voltage will be

$$V_t = V_{tf} + V_{th} \tag{9}$$

where V_{tf} is the fundamental component and V_{th} is the harmonic component of the terminal voltage. The fundamental component can be obtained as given in [3] and the harmonic components can be obtained by extracting the fundamental component from the original signal.

The system response (i.e. Load voltage) with the non-linear load along with the balanced load during sag and after sag with & without compensator is shown in Fig. 6. It has been observed that it contains high frequency harmonics due to non-linear load. Hence to provide a low impedance path for these high frequency harmonics currents we use a filter capacitor C_f of appropriate value connected in shunt at PCC as shown in Fig. 7.

It has been observed that the large value of filter capacitor C_f is unable to compensate the sag and the high frequency harmonics and spikes. Hence it is always suggested to use the low value of C_f which provides the better compensation to harmonic contents. It is seen that in this configuration DVR injects the required voltage with proper phase angle in order to compensate distorted sag & to cancel the negative and zero sequence components in load voltages to provide balanced load voltage.

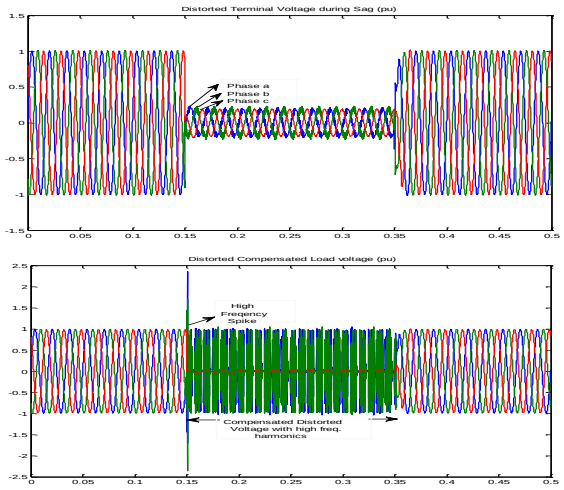

Figure 6. Distorted voltage during sag, compensated load voltage without filter capacitor in shunt at PCC.

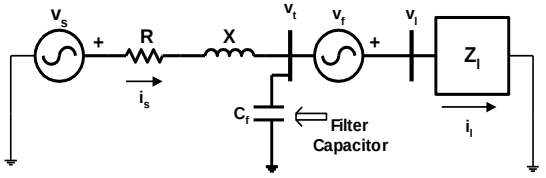

Figure 7. DVR configuration with shunt filter capacitor at PCC.

The DVR power given by (10) is oscillating with a mean of zero as shown in Fig. 8.

$$P_{fav} = V_{fa}i_{sa} + V_{fb}i_{sb} + V_{fc}i_{sc} \quad (10)$$

Case 3: Filter capacitors in shunt with PCC and Load.

With DVR configuration suggested in case-2, load voltage still contains harmonics & hence DVR configuration is further modified by putting additional filter capacitor C_d shunted at load as shown in fig. 9. The shunt connected capacitor across the load provides an alternate path for high frequency switching components in the load voltage and make it balanced sinusoidal. The compensated load voltage with reduced harmonics for the DVR configuration suggested in case-3 is as shown in Fig. 10.

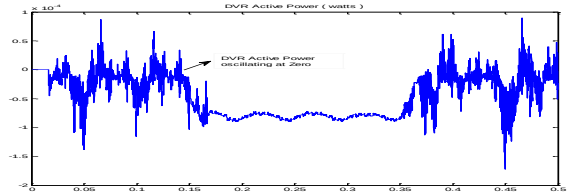

Figure 8. Compensated load voltages, DVR power & DVR injected power.

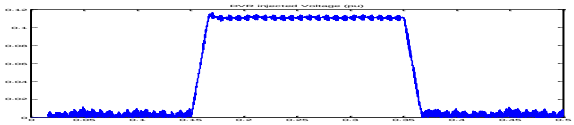

Figure 9. Single phase equivalent circuit of DVR with filter capacitor in shunt at PCC and load.

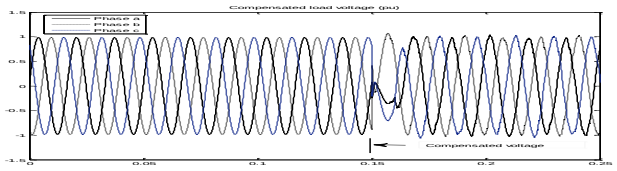

Figure 10. Compensated Load voltages with high frequency switching components for case-3.

V. Performance Evaluation

The performance of DVR with different configurations is evaluated for different loads. It has been observed that when the DVR with filter capacitor connected in shunt is used for compensating the balanced linear RL load, the system shows the satisfactory results and maintains the load & terminal voltage at 1.0 pu. In this case it is seen that the load voltage is settle down ≈ 1.0 pu. Since the system operates in steady state DVR does not supply or absorb any active power. The load voltage shows only positive sequence component, since the negative & zero sequence components has been canceled by DVR. Also it shows satisfactory active & reactive power across load.

When the system is tested with non-linear load in addition to the balanced linear load and with the slight modification in the DVR configuration (a filter capacitor in shunt with PCC).It is seen that the high frequency harmonics are still present in load voltage & cannot be removed completely. Hence system performance is verified with an alternate modified DVR configuration (a filter capacitor in shunt with load) and it is observed that the load voltage is compensated to 1.0 pu.,with reduced harmonics & the DVR power still oscillates with a mean of zero.

VI. Sag Detector & Sag Corrector

The sag detector detects the presence of voltage sag & activates the control system for sag correction. The output SD is a pulse that is active as long as voltage is out of tolerance during the sag. The input voltages measured on the Vs source side are converted to dqo space vectors in synchronously rotating frame since they have faster response time as they are based on instantaneous quantities. The per unit magnitude of this space vector is compared to a reference value 0.9. It has been observed that it provides sufficiently accurate result for the sag.

A proportional feedback controller for voltage sag correction is used. The output T_{SAG} is a negative torque command to the control system. T_{SAG} is scaled error of the difference between per unit magnitude of the V_S voltage space vector measured & the reference value 1.0 pu. T_{SAG} value is limited by amount of energy available for discharge and stability conditions of the energy storage system. A detailed analysis of this will be a future work. A simple limiter is used for limiting the maximum and minimum value of the negative torque output.

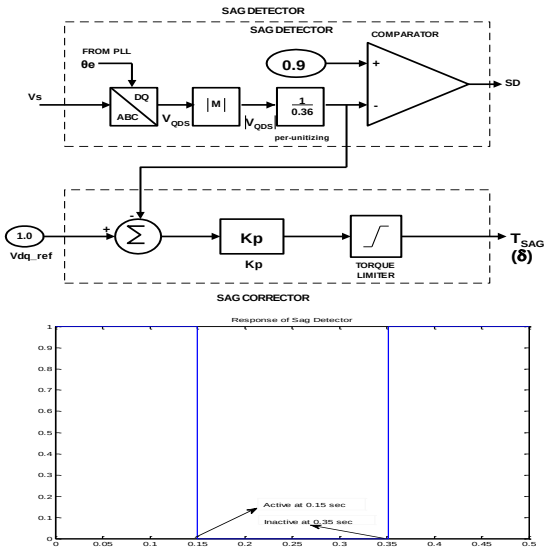

Figure 11. Sag detector & sag corrector layout, sag detector pulse response.

The sag detector & sag corrector circuit with the sag detector pulse response is shown is as shown in Fig. 11.

VII. Conclusion

These papers discuss the different configurations of DVR. It is seen that when load is balanced linear, the DVR along with filter capacitor is quite able to compensate the load voltage & terminal voltage. When the non-linear load is connected in addition to balanced linear RL load, the DVR with shunt filter capacitor at PCC is not able to suppress the harmonics & voltage spikes. Hence a low impedance path must be provided through a alternate additional shunt filter capacitor across load. It is seen that harmonics gets almost removed, load

voltages are compensated at 1.0 pu. with DVR power oscillating at zero. It is seen that among all the configurations case-3 gives the best performance. The selection of value of filter capacitors is very crucial and hence it must be chose judiciously.

APPENDIX

System parameters:

System voltage	:	480 V.
Feeder impedance	:	0.2 + j0.377 Ω
Load impedance	:	5 + j3.7704 Ω
DC Capacitor Voltage	:	400 V
Fault impedance	:	0.3 Ω
Non-linear rectifier load	:	1 + 0.003377 Ω
Filter capacitance	:	20 uF

REFERENCES

[1] M. H. Bollen, *Understanding Power Quality Problems: Voltage Sag & Interruption*, 2nd ed., John Wiley, IEEE Press 2000, ch. 4, pp. 139-252.

[2] A. Ghosh, *Power Quality Enhancement Using Custom Power Devices*, Norwell, MA: Kluwer Publications, 2002.

[3] A. Ghosh, A. K. Jindal, and A. Joshi, " Design of a capacitor-supported Dynamic Voltage Restorer (dvr) for unbalanced and distorted loads," *IEEE Trans. on Power Delivery*, vol. 19, no.1, pp. 405-413, January 2004.

[4] R. S. Weissbach, G. G. Karady, and R. G. Farmer, "Dynamic voltage compensation on distribution feeders using flywheel energy storage," *IEEE Trans. on Power Delivery*, vol. 14, pp. 465-471, Apr. 1999.

[5] H. J. Jung, I. Y. Suh, B. S. Kim, R. Y. Choi, and J. H. Song, "A study on DVR for unbalanced voltage compensation," in *Proc. IEEE Appl. Power Electron. Conf.*, 2002, vol. 2, pp. 1068-1073.

[6] S. S. Choi, B. H. Li, and D. M. Vilathgamuwa, "Dynamic voltage restoration with minimum energy injection," *IEEE Trans. on Power Delivery*, vol. 15, no. 1, February 2000.

[7] R. S. Weissbach, G. G. Karady, and R. G. Farmer, "A combined uninterruptible power supply and dynamic voltage restorer using a flywheel energy storage system," *IEEE Trans. on Power Delivery*, vol. 16, no. 2, Apr. 2001.

[8] F. Z. Peng, H. Akagi, and A. Nabae, "Compensation characteristics of the combined system of shunt passive and series active filters," *IEEE Trans. on Industry Applications*, vol. 29, no. 1, pp. 144–151, Jan/Feb 1993.

[9] B. K. Bose. *Modern Power Electronics & AC Drives*, Prentice hall, 2002.

[10] T. I. El-Shennawy, Abdel-Mon'em Moussa, M. A. El-Gammal, and A. Y. Abou-Ghazala, "A dynamic voltage restorer for voltage sag mitigation in refinery with induction motor load," *American Journal of Engineering and Applied Sciences*, vol. 3, no. 1, pp. 144-151, 2010.

[11] M. H. Haque, "Voltage sag correction by dynamic voltage restorer with minimum energy injection," *IEEE Power Engineering Review*, May 2000.

[12] T. Jimichi, H. Fujitam and H. Akagi, "A dynamic voltage restorer equipped with high-frequency isolated dc-dc converter," *IEEE Trans. on Industry Application*s, vol. 47, no. 1, Jan/Feb.2011.

S. P. Gawande reveiced his B.E. and M.Tech Degree in Electrical Engineering in 1999 and 2009 from Nagpur university, Nagpur, India. Currently he is working as an Assistant professor in Electrical Engineering Department of Yeshwantrao Chavan College of Engineering, Nagpur. He is currently pursuing Ph.D. Degree at Visvesvaraya National Institute of Technology, Nagpur, India.

His research interests include custom power devices, power electronics and FACTS applications to power system. Mr. Gawande is a member of IEI, India and life member of ISTE.

M. R. Ramteke passed his AMIE (Electrical Engineering) Examination of Institute of Engineers (India) in 1988 and received M-Tech. (Electronics Engineering) & Ph.D. (Electrical Engineering) from Nagpur university, Nagpur (India) in 1994 and 2008 respectively**.** He is currently working as an Associate Professor in Electrical Engineering Department of Visvesvaraya National Institute of Technology (VNIT) Nagpur. India.

He has 15 years of experience in the field of teaching and research. His research interests include power electronics, resonant converters, FACTS devices and power quality.