IO Standard Based Low Power Design of RAM and Implementation on FPGA

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***Abstract*—In this work, we are applying different LVCMOS based IO standard in the target design and maintain same drive strength for low power design. Spartan-3 is 90-nm FPGA, on which we implement our circuit to re-assure power reduction in memory design. Here, drive strength is 8mA uniform. Power consumption is increasing with LVCMOS12 than the power consumption with LVCMO25 when frequency is higher than 1GHz. Power consumption is decreasing with LVCMOS12 than the power consumption with LVCMO25 when frequency is lower than 1GHz. 1 GHz is a threshold on which there is change in behavior of power dissipation. There is 18.81% power reduction achieved when memory is operating with 1GHz clock frequency. Current is maximum 1.681A on 1 THz and current is minimum i.e. 0.026A on 1 MHz clock frequency.**

***Index Terms*—LVCMOS, dynamic power, IO standard, RAM, drive strength, frequency.**

I. Introduction

LVCMOS is Low Voltage Complementary Metal Oxide semiconductor based IO standards. This IO standard has different variety LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25 and LVCMOS33. LVCMOS15, LVCMOS25 takes 1.2V and 2.5V output driver voltage respectively. Internal supply voltage of FPGA is 1.2V and auxiliary supply voltage is 2.5V.

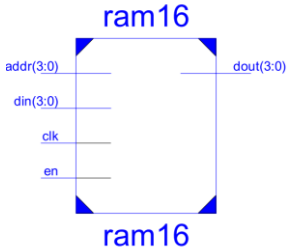

Figure 1. Top level schematic of RAM16

RAM has 4 inputs (addr, din, clock, and en) and one output (dout) as shown in Fig. 1. Address and Data input are of 4-bit width. Clk and enable is 1-bit input. When enable is high, RAM is in write mode. When enable is low, RAM is in read mode.

II. Literature Review

According to Reference [1], there is significant progress made by Behavioral synthesis tools in compiling hardware description language (HDL) programs into native generic register (NGR) format or RTL specifications. It is necessary to manually write code in order to use optimal resources in memory system optimization. Different automated memory optimization techniques have been proposed in recent years, such as data reuse and memory partitioning [1], but the integration problem is a challenge. Reference [1] shown FPGA behavioral synthesis is possible with integrating data reuse, loop pipelining, memory partitioning, and memory merging into an automated optimization flow (AMO). Reference [1] also develops memory padding to enhance memory partitioning of indices with mod operations. Experimental results on Xilinx Virtex-6 FPGAs show that integrated approach [1] can gain an average 5.8x throughput and 4.55x latency improvement compared to the approach without memory partitioning. Moreover, memory merging saves up to 44.32% of block RAM (BRAM). Reference [2] achieves 35.9% dynamic power reduction and 36.11% dynamic current reduction by shifting drive strength from 24mA to 2mA on LVCMOS25 when 2.5 V is output driver supply voltage and 1.0V is input supply voltage. [2] Also achieve 30% dynamic power reduction and 21.7% dynamic current reduction by shifting drive strength from 24mA to 2mA on LVCMOS12 when 1.2V is output driver supply voltage. In [3], a bus design techniques to achieve impedance matching and power distribution is described. In contrast to conventional schemes, the scheme in [3] is flexible to accept variance in the line impedance of each segment of the bus, and the impedance-matching resistance values are determined accordingly, in these way higher degrees of freedom for optimization is possible. General formulas of the optimal line impedances and matching resistances are derived in [3]. In [3], the ratios of master driver and branch receivers in term of power and voltage are also validated and verified, showing that these ratios are dependent on the branch number and master-to-branch impedance. Similar relations are also derived in [4] for the backward direction. Reference [4] provides a performance analysis of energy efficient and high performance Look up Table (LUT) with circuit technique. Proper sizing of each and every sleep transistors of LUT are done [4] to achieve an optimum power and energy delay relationship so that it

Manuscript received January 5, 2013; revised May 7, 2013.

doi: 10.12720/joace.1.4.316-320

can be used for fast growing energy efficient applications. In reference [5], digitally controlled impedance IO Standard is used in memory interface design. In [5], 50% dynamic power reduction at 1.5V output driver voltage, 35.2% dynamic power reduction at 1.8V output driver voltage in comparison to 2.5V output driver voltage in DCI based IO standard is achieved. In reference [6], there is 81.19%, 92.05% dynamic power reduction when using LVCMOS12 in place of HSTL_II_18 and SSTL2_I_DCI respectively. Reference [6] also achieved 65.56%, 72.59% and 73.41% dynamic power reduction in ALU with LVDCI IO standard in place of LVDCI_DV2, HSTL_I, and LVCMOS12 respectively. There is 68.34% and 52.51% dynamic power reduction in ALU in [6] when using LVCMOS12 and LVCMOS15 in place of LVCMOS25. There is 62.45% dynamic power reduction in ALU, when we use HSTL_I in place of SSTL2_I_DCI in [6].

III. Power Analysis of 4-bit RAM

A. Power is Inversely Proportional to Clock Period

We know that,

$$P \alpha 1/T \quad (1)$$

and

$$P \alpha f \quad (2)$$

From Equation 1 and 2, total power decrease with increase in clock period and decrease in frequency. When using default IO standard LVCMOS25, at 1 ns clock period, total power is 101mW. At 10 ns clock period, total power reduce to 83mW. At 100 ns clock period, total power reduce to 0.081mW finally as shown in Table I. At 10GHz clock frequency, total power is 278mW. At 100 GHz, total power is 2067mW. At 1THz clock frequency, total power reduce to 19.616W finally.

TABLE I. Power Dissipation Using LVCMOS25 IOs Standard

Frequency	Clocks Power	Leakage Power	Dynamic Power	Total Power
1THz	16.276	0.125	19.491	19.616
100GHz	1.628	0.118	1.949	2.067
10GHz	0.163	0.084	0.195	0.278
1GHz	0.016	0.081	0.019	0.101
100MHz	0.002	0.081	0.002	0.083
10MHz	0.000	0.081	0.000	0.081

Power dissipation is listed in Table I, when we use LVCMOS25 IO standards.

B. Power is Directly Proportional to Frequency

TABLE II. Power Dissipation Using LVCMOS12 IOs Standard

Frequency	Clocks Power	Leakage Power	Dynamic Power	Total Power
1THz	16.276	0.122	22.247	22.370
100GHz	1.628	0.122	2.226	2.349
10GHz	0.163	0.081	0.224	0.305
1GHz	0.016	0.078	0.004	0.082
100MHz	0.002	0.078	0.004	0.082
10MHz	0.000	0.078	0.002	0.081

Power dissipation is listed in Table II, when we use LVCMOS12 IO standards.

C. Flow of Current in Device on Different Frequency

We know that, Current = Power/Voltage; current is directly proportional to Power. Here, current will increase with increase in power. From our Studies in Table I-II,

$$I \alpha P \quad (3)$$

and we have,

$$P \alpha f \quad (2)$$

From (3) and (2), we have

$$I \alpha f \quad (4)$$

LVCMOS25 is using 2.5V output driver supply voltage, 2.5V auxiliary supply voltage for JTAG and configuration pin and 1.2V internal core supply voltage. Current Flow is listed in Table III when IO standard is LVCMOS25.

TABLE III. Current Flow in 90-nm Spartan-3 FPGA Using LVCMOS25

	Source	Voltage	Total current(A)	Dynamic current(A)
1MHz	V_{ccint}	1.200	0.026	0.000
	V_{ccaux}	2.500	0.018	0.000
	V_{cco25}	2.500	0.002	0.000
10MHz	V_{ccint}	1.200	0.026	0.000
	V_{ccaux}	2.500	0.018	0.000
	V_{cco25}	2.500	0.002	0.000
100MHz	V_{ccint}	1.200	0.027	0.002
	V_{ccaux}	2.500	0.018	0.000
	V_{cco25}	2.500	0.002	0.000
1GHz	V_{ccint}	1.200	0.042	0.016
	V_{ccaux}	2.500	0.018	0.000
	V_{CCO25}	2.500	0.002	0.000
10GHz	V_{ccint}	1.200	0.190	0.162
	V_{ccaux}	2.500	0.018	0.000
	V_{cco25}	2.500	0.002	0.000
100GHz	V_{ccint}	1.200	1.681	1.624
	V_{ccaux}	2.500	0.018	0.000
	V_{cco25}	2.500	0.002	0.000
1THz	V_{ccint}	1.200	1.681	1.624
	V_{ccaux}	2.500	0.018	0.000
	V_{cco25}	2.500	0.002	0.000

TABLE IV. Current Flow in 90-nm Spartan-3 FPGA Using LVCMOS12

	Source	Voltage	Total current(A)	Dynamic current(A)
10MHz	V_{ccint}	1.200	0.027	0.001
	V_{ccaux}	2.500	0.018	0.000
	V_{cco12}	1.200	0.003	0.001
100MHz	V_{ccint}	1.200	0.028	0.002
	V_{ccaux}	2.500	0.018	0.000
	V_{cco12}	1.200	0.003	0.001
1GHz	V_{ccint}	1.200	0.045	0.019
	V_{ccaux}	2.500	0.018	0.000
	V_{CCO12}	1.200	0.003	0.001
100GHz	V_{ccint}	1.200	1.916	1.854
	V_{ccaux}	2.500	0.018	0.000
	V_{cco12}	1.200	0.003	0.001
1THz	V_{ccint}	1.200	18.601	18.358
	V_{ccaux}	2.500	0.018	0.000
	V_{cco12}	1.200	0.003	0.001

LVCMOS12 is using 1.2V output driver supply voltage, 2.5V auxiliary supply voltage for JTAG and configuration pin and 1.2V internal core supply voltage. Current Flow is listed in Table IV when IO standard is LVCMOS12.

The default I/O standard in Spartan-3 is LVCMOS25. Therefore, voltage source is 2.5V Vcco25. VCCAUX supplies power to JTAG and dedicated configuration pins. It is independent of VCCO. The VCCAUX value may or may not equal to the VCCO or VREF value in the same bank. If VCCAUX and VCCO are both 2.5V on the same bank, then both can be powered by the same supply. VCCAUX is required regardless of the I/O standard used. VBATT does not draw any current when VCCAUX is applied; thus, the battery can be removed or exchanged. Core voltage means that the FPGA is working on this voltage. The IO voltage is the voltage supported by FPGA IOs; we use them in the different IO standards. VCCINT means a core voltage input, we have to connect this pin on a specific voltage. Vref is an IO for specific IO voltage standards like BLVDS, GTLP or others. VIN is an input voltage on a user defined pins.

D. Current Flow through VCCO

The default I/O standard in virtex-6 is LVCMOS25. Therefore, output driver supply voltage is 2.5V i.e. Vcco25. If we use LVCMOS12, then it changes to 1.2V i.e. Vcco12. Table V shows the flow of current due to output driver supply voltage (VCCO).

TABLE V. CURRENT FLOW THROUGH VCCO

Frequency	Total Current		Dynamic Current	
	VCCO12	VCCO25	VCCO12	VCCO25
1MHz	0.003	0.002	0.000	0.001
10MHz	0.003	0.002	0.000	0.001
100MHz	0.003	0.002	0.000	0.001
1GHz	0.003	0.002	0.000	0.001
10GHz	0.003	0.002	0.000	0.001
100GHz	0.003	0.002	0.000	0.001
1THz	0.003	0.002	0.000	0.001

E. Current Flow due to Auxiliary Supply Voltage

TABLE VI. CURRENT FLOW THROUGH VCCAUX

Frequency	Total Current	Dynamic Current
1MHz	0.018	0.000
10MHz	0.018	0.000
100MHz	0.018	0.000
1GHz	0.018	0.000
10GHz	0.018	0.000
100GHz	0.018	0.000
1THz	0.018	0.000

VCCAUX supplies power to JTAG and dedicated configuration pins. It is independent of VCCO. The VCCAUX value may or may not equal to the VCCO or VREF value in the same bank. If VCCAUX and VCCO are both 2.5V on the same bank, then both can be powered by the same supply. VCCAUX is required regardless of the I/O standard used. VBATT does not draw any current when VCCAUX is applied; thus, the battery can be removed or exchanged. Table VI shows the flow of current due to auxiliary supply voltage (VCCO). Current flow due to VCCAUX is uniform and independent of clock frequency on which we operate our device as listed is Table VI.

F. Current Flow due to Core Supply Input Voltage

TABLE VII. CURRENT FLOW THROUGH VCCINT

Frequency	Total Current	Dynamic Current
1MHz	0.026	0.000
10MHz	0.026	0.000
100MHz	0.027	0.002
1GHz	0.042	0.016
10GHz	0.190	0.162
100GHz	1.681	1.624
1THz	1.681	1.624

Current flow due to internal supply voltage is dependent on frequency. Change in current with change in frequency is listed in Table VII. Current is maximum 1.681A on 1 THz and current is minimum i.e. 0.026A on 1 MHz clock frequency. Core voltage means that the FPGA is working on this voltage. The IO voltage is the voltage supported by FPGA IOs; we use them in the different IO standards. VCCINT means a core voltage input, we have to connect this pin on a specific voltage. Vref is an IO for specific IO voltage standards like BLVDS, GTLP or others. Vin is an input voltage on a user defined pins.

G. RTL Schematic of RAM

RTL is register-transfer level and is based on native generic register (NGR) file of target design. Fig. 2 shows the RTL schematic of the target design RAM. RTL schematic of this RAM has 1 16x4-bit single-port distributed RAM, 4 Registers, 4 Flip-Flops and 14 IOs.

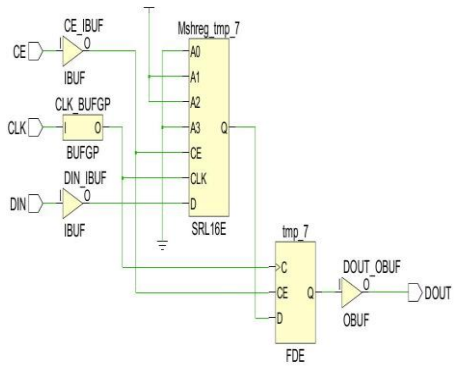

Figure 2. RTL schematic of RAM

H. Technology Schematic of RAM

The technology schematic of target design RAM is shown in Fig. 3. It has one Inverter, four flip-flops, four RAMs, one global clock buffer, nine input buffers and four output buffers.

All used components are listed in Table VIII. Technology schematic is based on native generic circuit (NGC) file of this design. This is using 3 slices out of

available 4656 slices in Spartan-3. This is using 4 flip-flops out of available 9312 flip-flops in Spartan-3. This is using 5 LUT4 out of available 9312 LUTs in Spartan-3. This is using 14 bonded IOBs out of available 232 bonded IOBs in Spartan-3. There is one global clock buffer is in use as shown in Fig. 3 and listed in Table VIII.

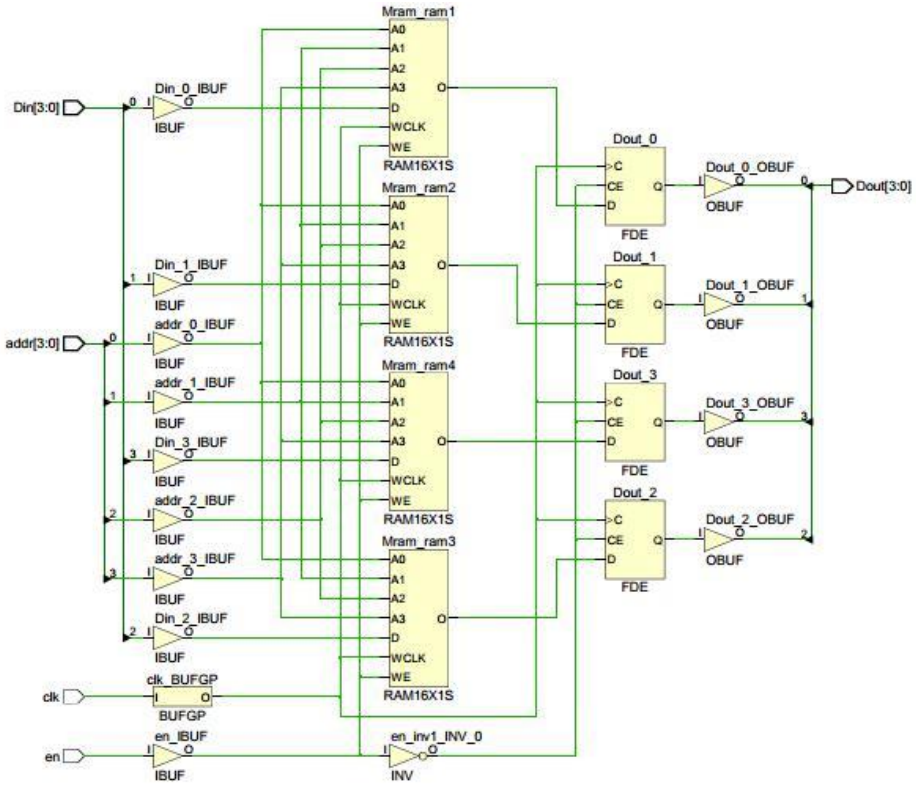

Figure 3. Technology schematic of RAM

TABLE VIII. CELL USAGE OF RAM IN 40-NM VIRTEX-6

Cell Usage of RAM		
Category	**Component Name**	**Number of Component**
BELS	Inverter	1
Flip-Flops/Latches	FDE	4
RAM	RAM16X1S	4
Clock Buffer	BUFGP	1
IO Buffer	IBUF	9
	OBUF	4

I. On Chip Resource Utilization in FPGA

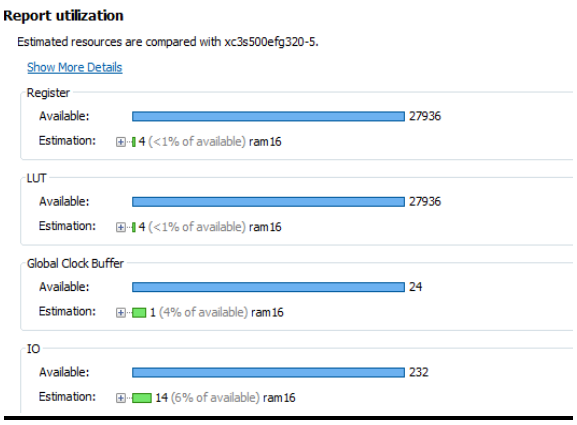

Figure 4. On-Chip resource utilization by memory

As per shown in Fig. 4, Memory is using 4 out of 27936 registers, 4 out of 2793 LUT, 1 out of 32 global clock buffers and 14 out of 232 IOs block available in Spartan-3 FPGA.

IV. CONCLUSION

In this work, we applied different LVCMOS based IO standard in the target design and maintain same 8mA drive strength. Power consumption is increasing with LVCMOS12 than the power consumption with LVCMO25 when frequency is higher than 1GHz. Power consumption is decreasing with LVCMOS12 than the power consumption with LVCMO25 when frequency is lower than 1GHz. 1 GHz is a threshold on which there is change in behavior of power dissipation. There is 18.81% power reduction achieved when memory is operating with 1GHz clock frequency. There is 18.81% power reduction achieved when memory is operating with 1GHz clock frequency. Current is maximum 1.681A on 1 THz and current is minimum i.e. 0.026A on 1 MHz clock frequency.

V. FUTURE SCOPE

We implemented this design on 90-nm Spartan-3 FPGA. We can implement this design on 40-nm Virtex-6 FPGA and 28-nm Virtex-7 FPGA. From the smallest target design four-bit RAM, we can proceed to larger memory in size of kilo byte (KB), megabyte (MB) and then reduce power consumption in significant amount. In this work, we work LVCMOS as IO standard; there is

scope to extent this work on other IO standard HSTL, SSTL and DCI.

ACKNOWLEDGMENT

The authors would like to thank Prof. S.G Deshmukh, Director ABV-IIITM for his research motivation and Support.

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