A High Speed-Low Power Comparator with Composite Cascode Pre-amplification for Oversampled ADCs

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***Abstract*—This paper presents a high speed- low power CMOS comparator using composite cascode differential pair as a pre-amplification stage. The purpose of this work is to design a comparator for oversampled ADC application. This comparator is designed using 180nm CMOS technology with a power supply of 1.2V. Pre and post layout simulation of the proposed circuit is done using cadence tool. The total power consumption of the comparator is 71.61µW and unity gain-bandwidth is 1GHz. The DC offset voltage is 12mV, gain is 70dB while total area occupied by comparator is 684µm^2. This design achieves an OSR (Oversampling Sampling Ratio) greater than 1000 which corresponds to SNR improvement of 30dB for Σ-Δ converters.**

***Index Terms*—high speed comparator, analog to digital convertor, composite cascode, oversampled ratio.**

I. Introduction

Analog to digital conversion is a key factor in any electronic system. The analog data is converted to digital data so that processing could be easy and storage of data can be possible. ADC is categorized into Nyquist rate ADC and oversampled ADC. Conventional Nyquist rate converters need analog components which must be highly immune to noise and interface, but oversampling converters can be designed using simple and high tolerance analog components.

Comparators play a very important role in analog to digital conversion for increasing the overall performance of the system. Usually in any ADC the comparator consumes most power of the core (e.g., in Flash type ADC for n bit resolution 2^n-1 number of comparators are needed). Hence intelligent design methodologies are highly needed for low power –reduced area design.

With miniaturization of circuit, the design of comparators for low supply voltages (less than 3.3V) is a challenging task. The main cause of problem in low voltage design is that threshold voltage and V_{DSAT} does not scale down with supply voltage or with smaller size technologies [1]. Numerous low voltage design techniques such as bulk driven, low voltage current mirrors, floating gates etc have been proposed by He et al. [2], Rajput et al. [3], and Yu et al. [4] respectively.

This work presents a high speed uncompensated comparator for sigma delta ADCs focused for audio applications. For high gain bandwidth we avoid compensation techniques as it causes degradation in bandwidth.

Section II and Section III discusses the proposed work and offset issues while section IV presents the simulation work. Conclusions are discussed in Section V.

II. Proposed Work

The modulator block diagram of the basic Σ-Δ modulator is shown in Fig. 1. It consists of an integrator, comparator and a digital to analog unit.

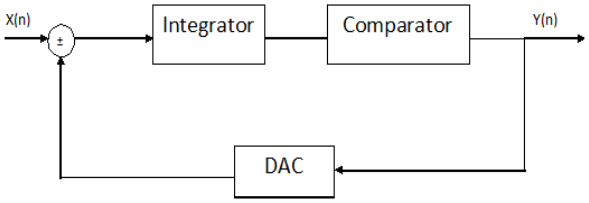

Figure 1. Basic Σ-Δ modulator

In Σ-Δ ADCs speed and resolution are complementary to each other. The block is followed by digital decimation filter to make complete Σ-Δ ADCs. The order of sigma delta modulator depends upon number of integrator. Σ-Δ ADCs uses one bit quantizer known as comparator. This block of Σ-Δ modulator is the main power consuming section of the modulator.

As the present work is designed for audio applications (bandwidth less than 25 kHz), hence to achieve an oversampling ratio >1000 the sampling frequency chosen is 50 MHz Moreover to design a Σ-Δ converter for these applications we need a high speed comparator which can work satisfactorily in this range and dissipate minimum power. The current work thus deals with efficient design of comparator and is designed using four stages as presented in Fig. 2.

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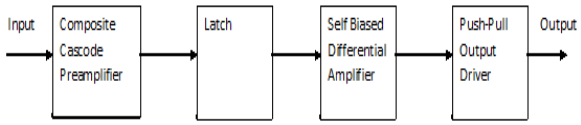

Figure 2. Architecture of proposed comparator

The various blocks are composite cascode preamplifier stage, latch stage, self biased differential amplifier stage & finally a push-pull output driver stage.

In conventional cascode structure, the gain is increased by increasing the output impedance. However the conventional cascode structure face limitations in low power and low voltage applications due to limited output swing & bias voltage requirement. The circuit performance thus degrades at low voltage. The main limitation faced in low voltage design is threshold voltage of transistor & noise level of device. The composite cascode circuit proposed by Comer et al. [5] is shown in Fig. 3. In this circuit the gate of transistor M1 & M2 are driven by same signal source & bias voltage.

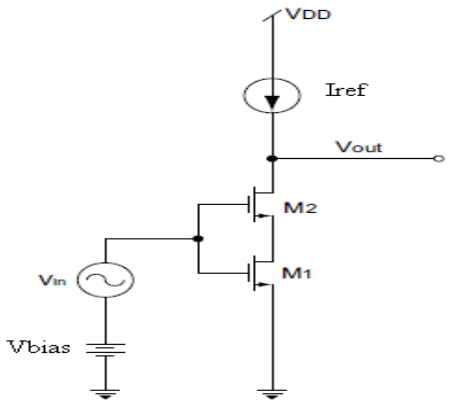

Figure 3. Basic composite cascode circuit [5]

This composite cascode stage has the following advantages over conventional cascode. First it reduces the bias headroom voltage required and second it provides higher output impedance at low bias current hence being more power efficient. Mean time it settles some devices in sub threshold region and other in the active region.

The region of operation of transistor in inversion region is defined in terms of normalization current I_f. If $I_f > 100$ then transistor operates in strong inversion region and if $I_f << 1$ then it operates in weak inversion region. The current I_f can be defined as [6]:

$$I_f = \frac{I_{ref}}{Is} \tag{1}$$

where,

$$Is = \mu C_{ox} \frac{\phi_t^2 W}{2L} \tag{2}$$

ϕ_t is thermal voltage & I_s is reverse saturation current. So if M2 is chosen with higher W/L than M1, with suitable V_{bias} & I_{ref} then M1 is placed in strong inversion region & M2 in weak inversion region. The gain is increased in this case due to weak inversion region at M2, however high capacitance will cause bandwidth to degrade.

The transistor level schematic of proposed circuit is shown in Fig. 4. In the composite cascode preamplifier, the transistors PM0 & PM1 operates in strong inversion region while the transistor PM2 & PM3 operates in weak inversion region. Transistors PM4, PM5, PM6 and PM7 form a current source and transistors NM0, NM1, NM2 and NM3 form a current sink. The sizing is done so that the output impedance of preamplifier stage can be increased. The current I_1 decides the unity gain bandwidth of preamplifier stage. The gain of preamplifier stage is 43dB and the gain bandwidth is 1GHz.

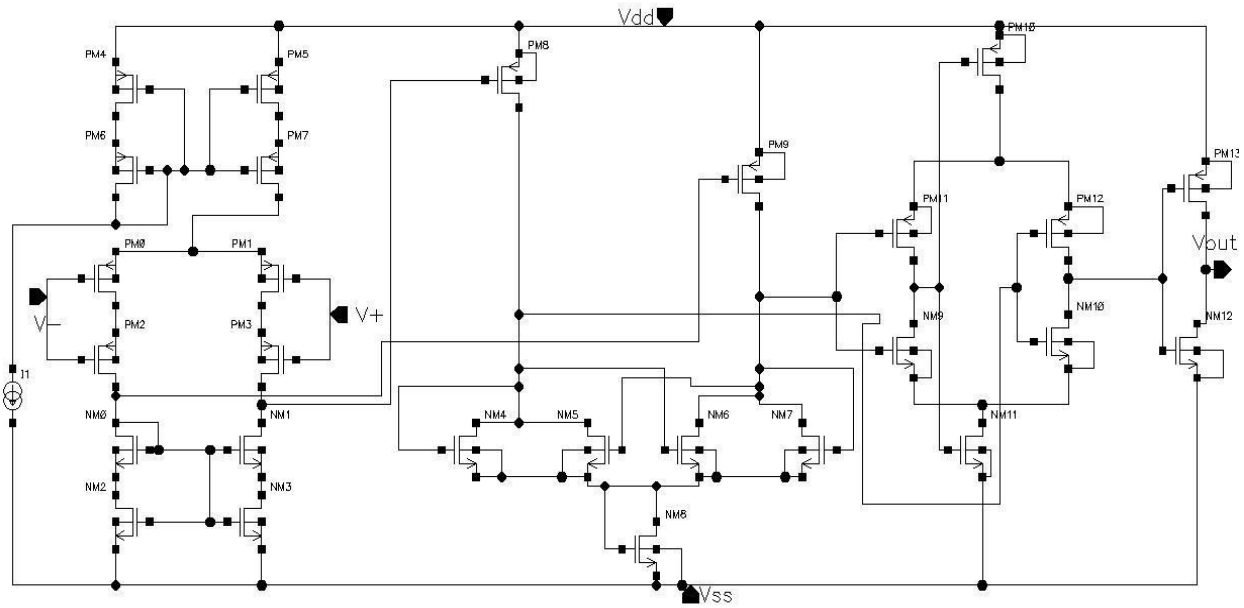

Figure 4. Schematic of proposed comparator

The second stage of Fig. 4 is a latch circuit formed by the cross coupled NMOS pair NM5 and NM6. The output of preamplifier acts as input of latch. The main cause of offset in preamplifier-latch configuration is due to offset in preamplifier stage and in latch stage. The offset of preamplifier-latch comparator is made of two parts:

- Offset Vos1 is caused by the input transistor mismatch of preamplifier and process variation while
- Offset Vos2 is caused by the mismatch in transistor pair NM5 and NM6 of latch circuit.

The analysis of offset voltage Vos1 can be defined by the formula [7], [8]:

$$V_{os1} = S_{0p}^2 + S_{1p}^2 + S_{2p}^2 + S_{3p}^2 + S_L^2 \quad (3)$$

where S_{np} are the offset due to nth transistor in preamplifier and S_L is cumulative offset due to load transistors PM4, PM5, PM6 and PM7.

The total offset voltage [10] can therefore be defined as:

$$V_{os1} = V_{os1} + \frac{V_{os2}}{2} \quad (4)$$

The latch is followed by a circuit which can quickly generate large amount of current so that a significant amount of output capacitance can be driven in a very short time. The latch comparator output drives a self biased differential pair and output of self biased differential pair drives push pull stage.

III. Dynamic DC Offset

The corresponding DC characteristic (shift in dc characteristic is known as offset) of comparator is invoked. To yield the variance of input offset voltage, statistical techniques (Monte Carlo simulations) is also carried out. This simulation result (put up in later section) shows the percentage of offset voltage due to transistor mismatch and process variation.

There are three sources of offset voltage in comparator.

- First mismatch between input differential pair of PMOS (pairs PM0/PM1 and PM2/PM3).
- Second mismatch is in the transistor of latch stage and
- Third is due to process variation.

The following equation gives the random mismatch in threshold voltage (δ_{Vth}) of transistor pair [9]:

$$\delta_{Vth}^2 = \frac{A_{Vth}^2}{WL} + S_{V0}^2 \cdot D^2 \quad (5)$$

where A_{Vth} is defined as process dependent parameter, L and W are length and width of transistor pair respectively, D is distance between transistor pair in its layout while S_{V0} is variation of V_{T0}.

IV. Simulation Results

The DC characteristic curve for the comparator is shown in Fig. 5. These results are obtained from Spectre simulation for 180nm CMOS technology with 1.2V single ended power supply.

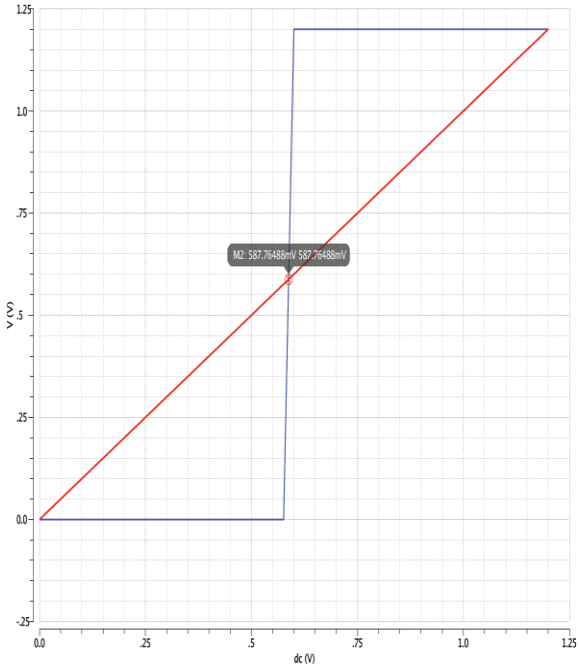

Figure 5. The DC characteristic of comparator

The dc characteristic shows an offset voltage of 12mV and the gain of comparator as 70dB. The unity gain bandwidth obtained is 1GHz. The transient response of the high speed comparator is presented in Fig. 6.

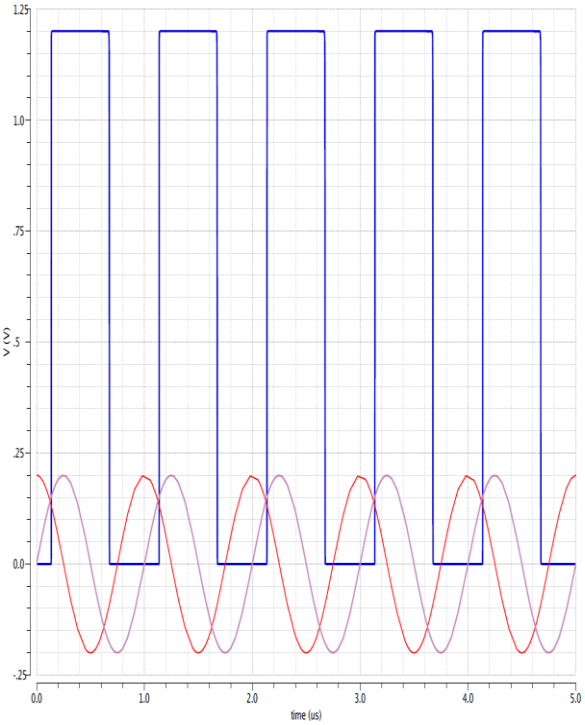

Figure 6. Transient response of comparator

The propagation delay τ_{PHL} for the proposed circuit is 11ns and propagation delay τ_{PLH} is 8ns.

For the statistical analysis of probability distribution of offset voltage, Monte Carlo simulation is carried out and the results are presented in Fig. 7, Fig. 8, Fig. 9 and Fig. 10.

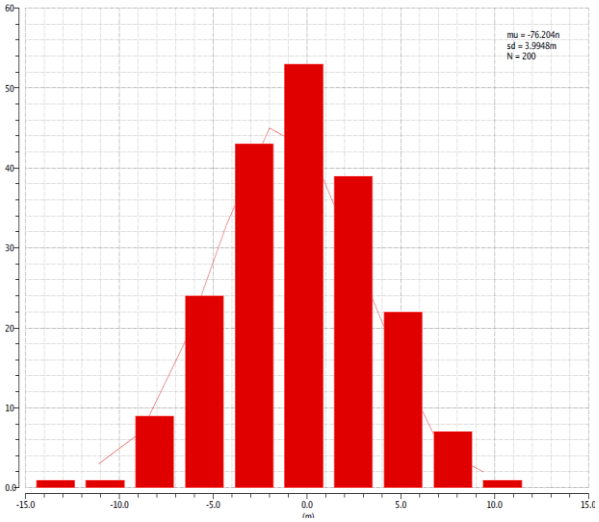

Figure 7. The histogram of offset voltage due to mismatch of PM0/PM1

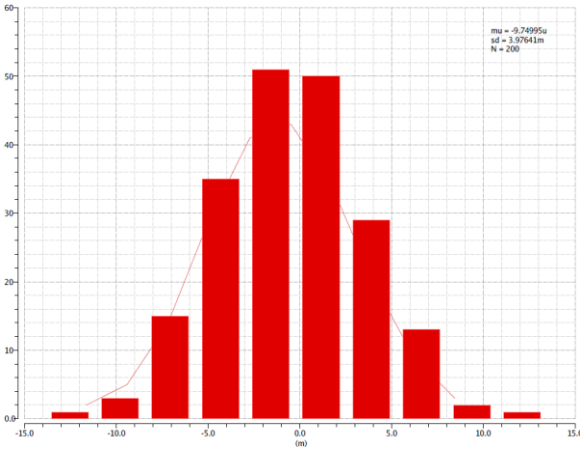

Figure 8. The histogram of offset voltage due to mismatch of PM2/PM3

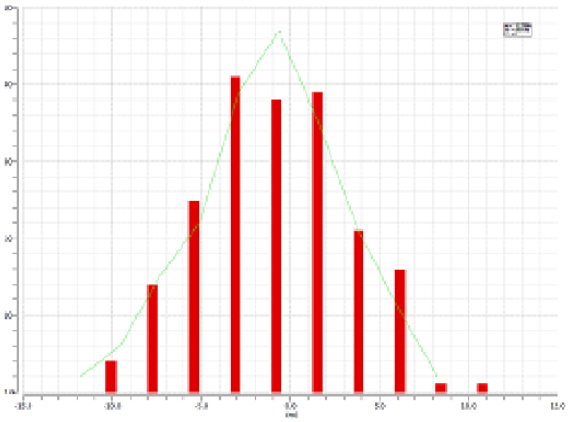

Figure 9. The histogram of offset voltage due to mismatch of NM5/NM6

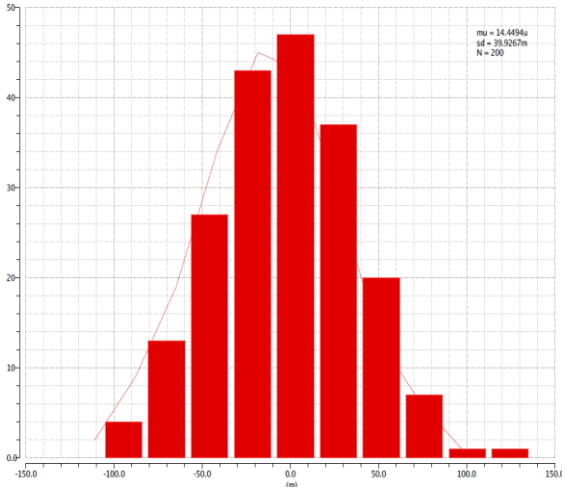

Figure 10. The histogram of offset voltage due to process variation

The offset voltages due to mismatch in different pairs and due to process variation are presented in Table I.

TABLE I. MONTE CARLO SIMULATION RESULT OF VOLTAGE OFFSET

Offset Due To	**Standard Deviation of Offset**
PM13/PM15	3.99480mV
PM14/PM12	3.97641mV
NM5/NM6	4.09317mV
Process Variation	39.9267mV

From Table-I it is clear that process variation is dominating the power spectral density of offset. However due to mismatch between the transistor pair it is about 4mV. The layout of the proposed comparator is also done on Cadence tool and is presented in Fig. 11.

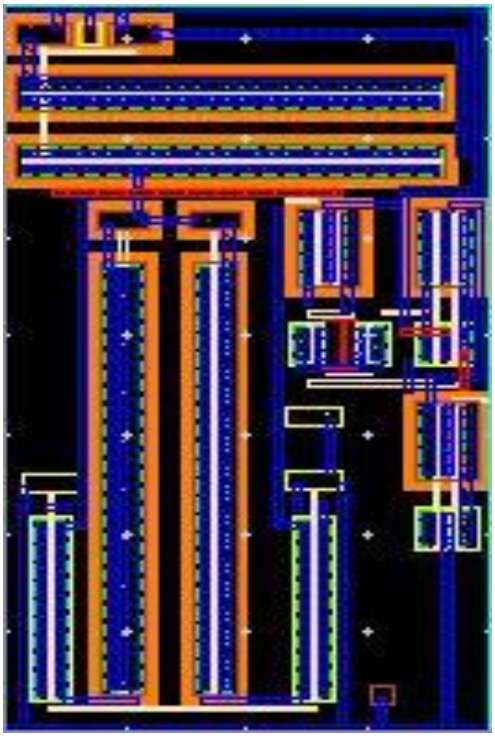

Figure 11. Layout of proposed comparator

V. Conclusion

A comparison of proposed comparator with different comparators is presented in Table II. The result shows that the proposed circuit dissipates minimum power and addresses the offset issue efficiently. For audio application the proposed circuit is highly suitable.

TABLE II. Performance Summary and Comparison

Author Name & Year	**Yang, 2007 [10]**	**Fahmy, 2010 [11]**	**Oliveria, 2007 [12]**	**This Paper**
Technology (µm)	0.35	0.18	0.13	0.18
Supply Voltage (V)	5	1.2	1.2	1.2
Power (µW)	490	246	142	71.61
Bandwidth	100 MHz	1 GHz	500 MHz	150 MHz
Area (µm2)	-	-	-	684
Offset (mV)	6.5	12.5	20.3	12

References

[1] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, IInd Ed., New York: Oxford University Press, 2004..

[2] R. He and L. Zhang, "Evalutation of modern MOSFET models for bulk driven applications," in *Proc. IEEE 51st Midwest Symp. on Circuits and Systems*, 2008, pp. 105-108.

[3] S. S. Rajput and S. S. Jamuar, "Low voltage, low power, high performance current mirror for portable analogue and mixed mode applications," in *Proc. IEEE Circuits, Devices and Systems*, vol. 148, 2002, pp. 273-278.

[4] C. G. Yu and R. L. Geiger, "Very low voltage operational amplifiers usign floating gate MOS transistor," in *IEEE Int. Symp. on Ciruits and Systems*, vol. 2, 1993, pp. 1152-1155.

[5] D. J. Comer, D. T. Comer, and C. Petrie, "The utillity of composite cascode on analog CMOS design," *Int. J.of Electronics*, vol. 91, no. 8, pp. 491-502, 2004.

[6] A. I. A. Cunha, M. C. Schneider, and C. Galup-Montoro, "An MOS transistor model for analog circuit design," *IEEE J. of Solid-State Circuits*, vol. 33, no. 10, pp 1510-1519, 1998.

[7] J. He, S. Zhan, D. Chen, and R. L. Geiger, "Analyses of static and dynamic random offset voltages in dynamic comparators," *IEEE Trans. on Circuits and System*, vol. 56, no. 5, pp. 911-919, 2009

[8] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, IVth Ed., John Wiley and Sons, Inc, New York, 2001.

[9] M. J. M. Pelgrom, A. C. J. Duninmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. of Solid State Circuits*, vol. 24, no. 5, pp. 1433-1439, 1989.

[10] W. R. Yang and J. D. Wang, "Design and analysis of a High-speed comparator in a piplined ADC," *Int. Symp. on High Density Packaging and Microsystems Integration*, 2007, pp. 1-3.

[11] G. A. Fahmy, R. K. Pokharel, H. Kanaya, and K. Yoshida, "A 1.2V 246µW CMOS latched comparator with neutralization technique for reducing kickback noise," in *Proc. IEEE Conf.*, 2010, pp. 1162-1165.

[12] J. P. Oliveria, J. Goes, B. Esperanca, N. Paulino, and J. Fernandes, "Low-power CMOS comparator with embedded amplification for ultra-high-speed ADCs," in *Proc. IEEE Int. Symp. on Circuits and Systems*, 2007, pp. 3602-3605.

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